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FEDERAL SUPREME COURT

IN THE NAME OF THE PEOPLE

JUDGMENT

X ZR 6/21

Delivered on:
January 10, 2023
Schönthal
Judicial Employee
as Clerk of the
Court

in the patent nullity case

ECLI:DE:BGH:2023:100123UXZR6.21.0

The X. Civil Senate of the Federal Supreme Court, at the oral hearing on January 10, 2023, by the Presiding Judge Dr. Bacher, Judges Hoffmann and Dr. Deichfuß, Judge Dr. Marx, and Judge Dr. Crummenerl

ruled:

On appeal by the defendant, the judgment of the 2nd Senate (Nullity Senate) of the Federal Supreme Court of October 22, 2020, is amended.

European patent 3 036 768 is declared partially invalid with effect for the Federal Republic of Germany by giving the patent claims the following wording:

1. A complementary metal oxide semiconductor, CMOS, device including a plurality of p-type metal oxide semiconductor, PMOS, transistors each having a PMOS drain and a plurality of n-type metal oxide semiconductor, NMOS, transistors each having an NMOS drain, comprising:

   at least three metal layers above the drains of the transistors, comprising a first metal layer, a second metal layer and a third metal layer; wherein the first metal layer is the lowest metal layer above the drains, the second metal layer is the next metal layer above the first metal layer and the third metal layer is the next metal layer above the second metal layer;

   a first interconnect on a first interconnect level on the first metal layer, connecting a first plurality of the PMOS drains together;

   a second interconnect on the first interconnect level connecting a second plurality of the PMOS drains together, the second plurality of the PMOS drains being different than the first plurality of the PMOS drains, the first interconnect and the second interconnect being disconnected on the first interconnect level;

   a third interconnect on the first interconnect level connecting a first plurality of the NMOS drains together; and

a fourth interconnect on the first interconnect level connecting a second plurality of the NMOS drains together, the second plurality of the NMOS drains being different than the first plurality of the NMOS drains, the third interconnect and the fourth interconnect being disconnected on the first interconnect level,

wherein the first interconnect, the second interconnect, the third interconnect, and the fourth interconnect are coupled together through at least one other interconnect level;

a fifth interconnect on a second interconnect level on the second metal layer, the fifth interconnect coupling the first interconnect and the second interconnect together; and

a sixth interconnect on the second interconnect level, the sixth interconnect coupling the third interconnect and the fourth interconnect together; and

a seventh interconnect on a third interconnect level on the third metal layer, the seventh interconnect coupling the fifth interconnect and the sixth interconnect together; and preferably wherein an output of the device is connected to the seventh interconnect.

2. The device of claim 1, wherein the first interconnect, the second interconnect, the third interconnect, and the fourth interconnect are each less than 2 μm in length.

3. The device of claim 1, wherein the fifth interconnect and the sixth interconnect are each less than 2 μm in length.

4. The device of claim 1, wherein the CMOS device is an inverter, the PMOS transistors each have a PMOS gate and a PMOS source, the NMOS transistors each have an NMOS gate and an NMOS source, the NMOS sources of the NMOS transistors being coupled together, the PMOS sources of the PMOS transistors being coupled together, the PMOS gates of the PMOS transistors and the NMOS gates of the NMOS transistors being coupled together.

5. The device of claim 1, further comprising:

a first set of interconnects on the interconnect level connecting different subsets of the PMOS drains together, the first set of interconnects including the first interconnect, the second interconnect, and one or more additional inter-

connects, each interconnect in the first set of interconnects being disconnected from other interconnects in the first set of interconnects on the interconnect level; and

a second set of interconnects on the interconnect level connecting different subsets of the NMOS drains together, the second set of interconnects including the third interconnect, the fourth interconnect, and one or more additional interconnects, each interconnect in the second set of interconnects being disconnected from other interconnects in the second set of interconnects on the interconnect level.

6. The device of claim 5, wherein each interconnect in the first set of interconnects and the second set of interconnects is less than 2 μm in length.

7. A method of laying out a complementary metal oxide semiconductor, CMOS, device including a plurality of p-type metal oxide semiconductor, PMOS, transistors each having a PMOS drain and a plurality of n-type metal oxide semiconductor, NMOS, transistors each having an NMOS drain,

the CMOS device including at least three metal layers above the drains of the transistors, comprising a first metal layer, a second metal layer and a third metal layer; wherein the first metal layer is the lowest metal layer above the drains, the second metal layer is the next metal layer above the first metal layer and the third metal layer is the next metal layer above the second metal layer,

the method comprising:

interconnecting a first plurality of PMOS drains with a first interconnect on a first interconnect level on the first metal layer;

interconnecting a second plurality of PMOS drains with a second interconnect on the first interconnect level, the second plurality of PMOS drains being disconnected from the first plurality of PMOS drains on the first interconnect level;

interconnecting a first plurality of NMOS drains with a third interconnect on the first interconnect level;

and interconnecting a second plurality of NMOS drains with a fourth interconnect on the first interconnect level, the second plurality of NMOS drains being disconnected

from the first plurality of NMOS drains on the first interconnect level, wherein the first interconnect, the second interconnect, the third interconnect, and the fourth interconnect are coupled together through at least one other interconnect level;

interconnecting the first interconnect and the second interconnect with a fifth interconnect on a second interconnect level on the second metal layer;

and interconnecting the third interconnect and the fourth interconnect with a sixth interconnect on the second interconnect level;

interconnecting the fifth interconnect and the sixth interconnect with a seventh interconnect on a third interconnect level on the third metal layer.

8. A method of operation of a complementary metal oxide semiconductor, CMOS, device including a plurality of p-type metal oxide semiconductor, PMOS, transistors each having a PMOS drain and a plurality of n-type metal oxide semiconductor, NMOS, transistors each having an NMOS drain,

the CMOS device including at least three metal layers above the drains of the transistors, comprising a first metal layer, a second metal layer and a third metal layer; wherein the first metal layer is the lowest metal layer above the drains, the second metal layer is the next metal layer above the first metal layer and the third metal layer is the next metal layer above the second metal layer,

the method comprising:

flowing a first current from a first plurality of PMOS drains interconnected with a first interconnect on a first interconnect level on the first metal layer;

flowing a second current from a second plurality of PMOS drains interconnected with a second interconnect on the first interconnect level, the second plurality of PMOS drains being disconnected from the first plurality of PMOS drains on the first interconnect level;

flowing a third current to a first plurality of NMOS drains interconnected with a third interconnect on the first interconnect level;

and flowing a fourth current to a second plurality of NMOS drains interconnected with a fourth interconnect on the

first interconnect level, the second plurality of NMOS drains being disconnected from the first plurality of NMOS drains on the first interconnect level,

wherein the first interconnect, the second interconnect, the third interconnect, and the fourth interconnect are coupled together through at least one other interconnect level, wherein the first current and the second current flows through said at least one other interconnect level to an output of the CMOS device upon the CMOS device receiving a low input, wherein the third current and the fourth current flows from the output of the CMOS device through said at least one other interconnect level upon the CMOS device receiving a high input;

wherein the first interconnect and the second interconnect are interconnected with a fifth interconnect on a second interconnect level on the second metal layer

and the third interconnect and the fourth interconnect are interconnected with a sixth interconnect on the second interconnect level;

wherein the fifth interconnect and the sixth interconnect are interconnected with a seventh interconnect on a third interconnect level on the third metal layer.

In all other respects, the action is dismissed.

The further appeal of the defendant and the appeal of the plaintiff re 1) are dismissed.

Of the costs of the appeal proceedings, the plaintiff re 1) shall bear 60% and the defendant 40%. The first-instance costs of the legal dispute are set aside against each other.

By law

Facts of the Case:

1 The defendant is the owner of European Patent 3 036 768 (patent in suit), which was granted with effect for the Federal Republic of Germany, was filed on August 21, 2014, claiming a U.S. priority of August 23, 2013, and relates to the structure of a semiconductor.

2 Claim 1, to which thirteen further claims are referred back, reads in procedural language:

> A complementary metal oxide semiconductor, CMOS, device including a plurality of p-type metal oxide semiconductor, PMOS, transistors each having a PMOS drain and a plurality of n-type metal oxide semiconductor, NMOS, transistors each having an NMOS drain, comprising:
> a first interconnect on an interconnect level connecting a first plurality of the PMOS drains together;
> a second interconnect on the interconnect level connecting a second plurality of the PMOS drains together, the second plurality of the PMOS drains being different than the first plurality of the PMOS drains, the first interconnect and the second interconnect being disconnected on the interconnect level;
> a third interconnect on the interconnect level connecting a first plurality of the NMOS drains together; and
> a fourth interconnect on the interconnect level connecting a second plurality of the NMOS drains together, the second plurality of the NMOS drains being different than the first plurality of the NMOS drains, the third interconnect and the fourth inter-connect being disconnected on the interconnect level, wherein the first interconnect, the second interconnect, the third interconnect, and the fourth interconnect are coupled together th[r]ough at least one other interconnect level.

3 Claim 14 protects a method of laying out, claim 15 a method of operation of such a semiconductor.

4 The plaintiffs claimed that the subject matter of the patent in suit was not patentable and went beyond the content of the application as originally filed. The defendant has defended the patent in suit as granted and with fifty-nine auxiliary requests in amended versions.

5 The Patent Court declared the patent in suit invalid insofar as its subject matter extended beyond the scope of the version newly defended at first instance by means of auxiliary request 3b'' (at second instance: auxiliary request 3a˝), and dismissed

the further claim. The plaintiff re 1) and the defendant appeal against this decision. The plaintiff re 1) (hereinafter: plaintiff) further seeks a complete declaration of invalidity of the patent in suit. The defendant opposes the appeal and defends with its appeal the patent in suit primarily in the version of the first instance auxiliary request 1 and in addition with sixty-two mostly new auxiliary requests.

Reasons for Decision:

6 Both appeals are admissible. The one of the defendant is partially well-founded.

7 I. The patent in suit relates to the construction of a device comprising a Complementary Metal Oxide Semiconductor (CMOS).

8 1. According to the description of the patent in suit, electromigration must be taken into account in the configuration of such a device.

9 Electromigration refers to the transport of material as a result of the gradual movement of ions in a conductor due to momentum transfer between conduction electrons and diffusing metal atoms. Electromigration reduces the reliability of integrated circuits because it can lead to loss of connections or circuit failure (para. 2).

10 To counteract this, U.S. application 5 903 019 provides for an aluminum line with a relatively large width for interconnected CMOS structures. US application 5 532 509 proposed a specific layout of transistors along a continuous conductive path (para. 3).

11 2. Against this background, the patent in suit concerns the technical problem of providing further possibilities for the construction of CMOS devices that take electromigration into account.

12 3. For solution, the patent in suit in the version of claim 1 defended by the main request proposes a CMOS device, the features of which can be structured as follows (changes compared to the granted version are highlighted):

1. A complementary metal oxide semiconductor (CMOS) device including (1.1 and 1.2) or comprising (1.3 to 1.13.1):

1.1 a plurality of p-type metal oxide semiconductor (PMOS) transistors, each having a PMOS drain;

1.2 a plurality of n-type metal oxide semiconductor (NMOS) transistors, each having an NMOS drain;

1.3 a first interconnect on an interconnect level connecting a first plurality of PMOS drains;

1.4 a second interconnect on an interconnect level connecting a second plurality of PMOS drains different from the first,

1.5 wherein the first interconnect and the second interconnect are not connected to each other on the interconnect level;

1.6 a third interconnect on the interconnect level connecting a first plurality of NMOS drains;

1.7 a fourth interconnect on the interconnect level connecting a second plurality of NMOS drains different from the first,

1.8 wherein the third interconnect and the fourth interconnect are not connected to each other on the interconnect level, and

1.9 the first interconnect, the second interconnect, the third interconnect and the fourth interconnect are coupled to each other by at least one other interconnect level;

1.11 a fifth interconnect on a second interconnect level, wherein the fifth interconnect couples the first interconnect and the second interconnect together;

1.12 a sixth interconnect on a second interconnect level, wherein the sixth interconnect couples the third interconnect and the fourth interconnect;

1.13 a seventh interconnect on a third interconnect level, wherein the seventh interconnect couples the fifth interconnect and the sixth interconnect to each other, and

1.13.1 preferably an output of the device is connected to the seventh interconnect.

13 4. Some features require explanation.

14 a) A CMOS device in the sense of feature 1 is a device comprising PMOS and NMOS transistors. However, claim 1 does not specify a particular switching logic.

15 aa) As an example of a CMOS device, the description of the patent in suit cites an inverter as shown schematically in Figure 1 reproduced below:

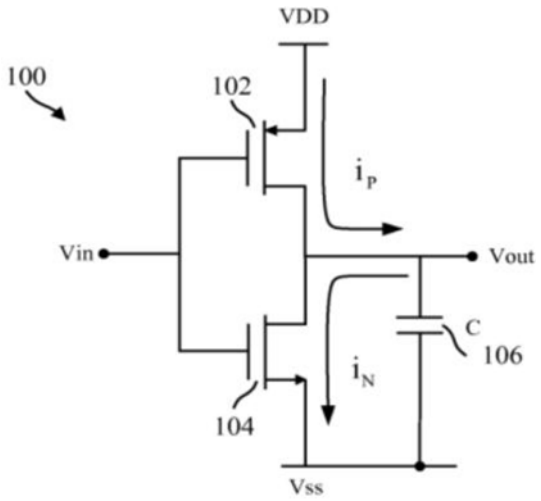


FIG. 1

16 The inverter comprises a PMOS transistor (102) and an NMOS transistor (104), whose gates and drains are connected to each other, respectively. The potential V_{DD} is applied to the source of the PMOS transistor (102), and the potential V_{SS} is applied to the source of the NMOS transistor (104). Depending on which potential V_{in} is applied to the two gates, one of the two transistors is conducting while the other is blocking. As a result, the output potential V_{out} at the two drains corresponds to either V_{DD} or V_{SS}. To allow a larger current flow, several such inverters can be connected in parallel (para. 16).

17 bb) As the Patent Court stated with reference to the reference book by Hütte (Das Ingenieurwissen, edited by Czichos and Hennecke, 32nd ed., 2004, B7, p. J21), other CMOS circuits were known in the prior art which have in common that an output can be connected via two paths with different potentials and for this purpose PMOS transistors are used on the high potential side and NMOS transistors on the low potential side.

18 cc) The Patent Court rightly concluded that claim 1 does not necessarily provide for a paired circuit of PMOS and NMOS transistors in which one transistor alternately conducts and the other blocks.

19 (1) According to the findings of the Patent Court, a device is already subsumed under the term CMOS technology if it comprises PMOS and NMOS transistors - irrespective of whether these transistors are used to implement CMOS logic.

20 The defendant does not point to any concrete evidence that would cast doubt on the completeness or correctness of these findings. On the contrary, the statements in B7 also speak in favor of their correctness.

21 B7 explains that for the circuits shown there, the effect of the two switches must always be opposite (complementary) to each other and that in CMOS technology MOS transistors with complementary function are used for this purpose. It can be seen from this that although CMOS technology is suitable for circuits of the type mentioned, its intended use is not limited to this.

22 (2) Against this background, the Patent Court rightly concluded from the fact that claim 1 does not contain any specifications for the switching logic that it is sufficient if the device is implemented in CMOS technology, while CMOS logic is not mandatory.

23 (3) The fact that the description of the patent in suit mentions different current flows, one of which occurs at high input potential and the other at low input potential (para. 8 aE), does not lead to a different assessment. This embodiment has not been reflected in claim 1.

24 (4) From the additional feature provided in the granted version of claim 15 (according to the second-instance main request: claim 8), according to which current flows to the PMOS drains at a low input level (low input) and to the NMOS drains at a high input level (high input), no deviating assessment results either.

25 As the plaintiff rightly asserts with reference to its first-instance argument, it also does not necessarily follow from this feature that CMOS logic must be present, because it is not specified in more detail at which point the input level is fed in.

26 b) Crucial to the desired reduction in the effects of electromigration are the arrangement and configuration of the interconnections of the PMOS and NMOS transistors across their drains.

27 Claim 1 as defended by main request provides for seven interconnects on three interconnect levels for this purpose.

28 aa) Interconnects between the drains are arranged on the first interconnect level.

29 (1) According to features 1.3, 1.4, 1.6 and 1.7, the PMOS and NMOS drains must in this case each be divided into (at least) two groups that are different from one another and are each connected to one another by their own interconnect.

30 According to features 1.5 and 1.8, the first and second interconnects (i.e., the two interconnects for PMOS drains) and the third and fourth interconnects (i.e., the two interconnects for NMOS drains) shall not be connected to each other.

31 (2) On the other hand, connections between a connection for PMOS and a connection for NMOS drains, for example between the first and third or between the second and fourth interconnects, are not excluded.

32 (a) Such compounds are used in the embodiment shown in Figures 9a and 9b reproduced below.

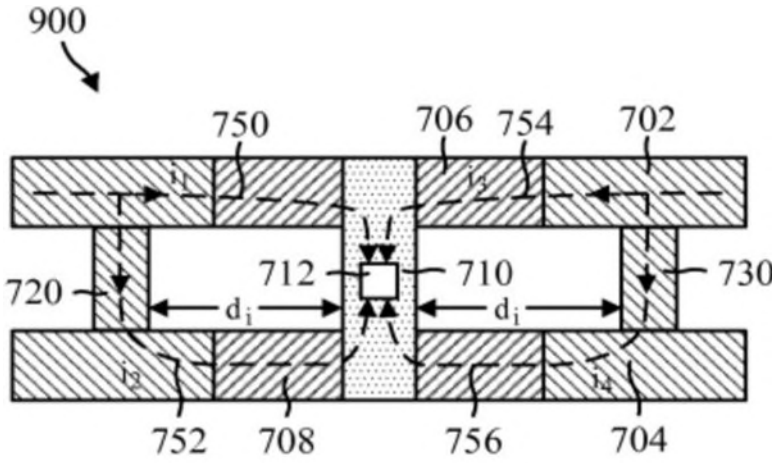


FIG. 9A

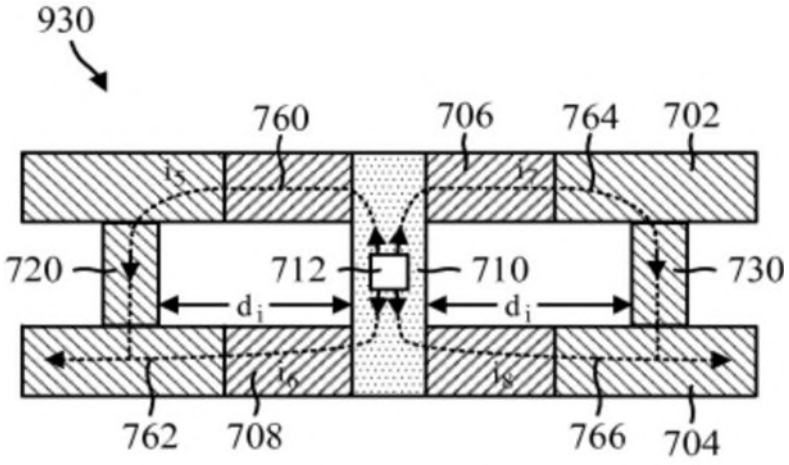


FIG. 9B

33 In this embodiment, the interconnect (702) arranged on a first metal level M1 and serving to interconnect PMOS drains and the interconnect (704) arranged on the same level and serving to interconnect NMOS drains are interconnected not only at higher levels (706, 708, 710), but also at the M1 level, via additional interconnects (720, 730, para. 34).

34 This ensures that a current flows through all connections arranged on the first level in both switching states, with a change of switching state leading to a reversal of the current direction. The latter counteracts wear due to electromigration (para. 35).

35 (b) Comparable interconnects are also provided in the embodiment shown in Figure 11 below.

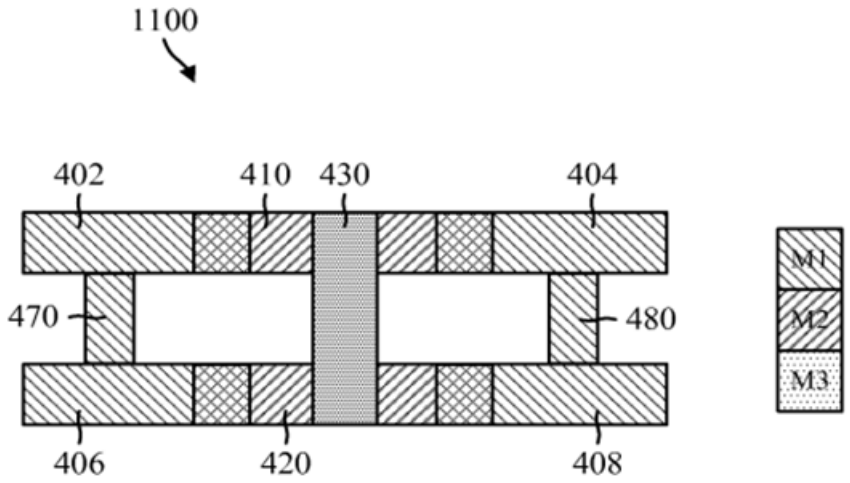


FIG. 11

36 This embodiment comprises two interconnects (402, 404) for PMOS transistors and two interconnects (406, 408) for NMOS transistors, all located on a first metal level M1.

The connections (402, 404) are not coupled to each other on the M1 level; the same applies to the connections (406, 408). The connections (402, 406), on the other hand, are coupled to each other at the M1 level by an interconnect (470). A corresponding interconnect (480) is arranged between the connections (404, 408). In this arrangement, interconnect lengths of less than two micrometers can be achieved. The interconnects (470, 480) open up parallel current paths and thus reduce the wear effect caused by electromigration (para. 38).

37 bb) The four interconnects of the first level are coupled to each other on at least one other interconnect level according to feature 1.9. How this is to be done is specified in features 1.11 to 1.13.

38 According to features 1.11 and 1.12, the first and second interconnects and the third and fourth interconnects must be coupled to each other by a further (the fifth and the sixth, respectively) interconnect. These two additional interconnects are located on a second interconnect level.

39 According to feature 1.3, the fifth and sixth interconnects must be coupled to each other via a seventh interconnect. This interconnect is located on a third interconnect level.

40 cc) According to the description of the patent in suit, the separation of the interconnects on the first level and the coupling on two further levels create the possibility to reduce the length of the interconnects, for example to a value of less than two micrometers. This makes it possible to increase the back stress and reduce the electromigration in the interconnects (para. 21 aE).

41 dd) Contrary to the view of the Patent Court, the fifth and the sixth interconnects may not run - not even partially - in the first interconnect level.

42 (1) A connection between the first and second interconnect and a connection between the third and fourth interconnect on the first interconnect level is explicitly excluded by features 1.5 and 1.8, respectively.

43 These features echo the embodiment described in the description of the patent in suit for two of three groups of embodiments.

44 In the explanations of Figures 3 to 6, which concern a first group of possible embodiments, it is emphasized throughout and several times that the interconnects for the individual groups of drains are not connected to each other on the metal level M1 and that coupling is only achieved with the aid of two further interconnects on a second level (paras. 21-31). Corresponding explanations are given with respect to Figures 11 to 13, which concern a third group of possible embodiments (paras. 38-42). This separation is expressly provided for in features 1.5 and 1.8.

45 In contrast, in the explanations to Figures 7 to 10, which concern a second group of possible embodiments, only one interconnect each is mentioned for PMOS and NMOS drains on the first metal level M1 (paras. 32-37). Even if it were to be inferred from this that there need only be one interconnect on the first level for each type of drain, or that several such interconnects need not be separated on the first level, this would have no significance for the interpretation of claim 1. Claim 1

explicitly provides for such a separation in connection with the other embodiments. It can be inferred from this that other embodiments must also have this configuration.

46 (2) In conjunction with features 1.5 and 1.8, features 1.11 and 1.12 specify in spatial and physical terms that the fifth and sixth interconnects are not assigned to the first but to the second interconnect level and accordingly couple the first and second or third and fourth interconnects there. This rules out configurations in which the first interconnect level is included in the coupling in partial sections.

47 Contrary to the plaintiff's view, the fact that in such a configuration without the participation of the subsections located in the second interconnect level a coupling does not take place on the first interconnect level does not justify a different consideration. This does not change the fact that the subsections located on the first interconnect level necessarily participate in the coupling with the consequence that, with regard to the function of the coupling, a clear assignment of the fifth and sixth interconnect to the second interconnect level is no longer possible.

48 (3) Contrary to plaintiff's view, the fact that features 1.5 and 1.8 refer to connecting, whereas features 1.11 to 1.13 refer to coupling, does not lead to a different assessment.

49 Neither from the description of the patent in suit nor from other circumstances are there any indications that the different choice of words is intended to express different technical effects. It merely serves to clarify the repeatedly emphasized circumstance that the individual interconnects are not connected with each other on the first level and that their coupling only takes place on a higher level.

50 (4) Contrary to the opinion of the Patent Court, feature 1.9 also does not result in a different assessment.

51 However, as the Patent Court correctly assumed in the approach, it follows from feature 1.9 that the coupling between the first four interconnects can take place on several levels. As already stated above in connection with Figures 9 and 11, connections on the first level are also considered here, for example between the first and the third interconnect. However, for the first and the second connection as well as for the third and the fourth connection, features 1.5 and 1.8 explicitly exclude a connection - consequently also a coupling - in the first level. This prohibition is neither removed nor relativized by feature 1.9.

52 5. The claims directed to the protection of an arrangement or operating method (in the version of the second-instance main request: claims 7 and 8) are essentially characterized by the device features from claim 1 and are not subject to any deviating assessment.

53 II. The Patent Court gave the following main reasons for its decision, insofar as it is still of interest in the appeal proceedings:

54 The subject-matter of the granted claim 1 was not new compared to US patent 5 444 276 (K8), US patent applications 2005/0212562 A1 (K9) and 2012/0221759 (K5), and European application 2 738 806 (K6). The obvious pre-used chip RF 6560 also anticipates the subject matter. The subject-matter of the first-instance auxiliary request 1 (i.e., of the second-instance main request) is also not new compared to the prior use and is suggested by K9.

55 K9 deals with the formation of driver cells of an ASIC as shown in Figure 12. The structure consists of two inverters, each formed by three PMOS and NMOS

transistors. The transistors are wired in three levels, which are designated Metal i-1, Metal i and Metal i+1. In the Metal i-1 layer, all gates are connected on both sides and the sources are connected to either the VDD potential for the PMOS transistors or VSS for the NMOS transistors. In addition, the drains would be connected. The connection extends in each case from the drain of the uppermost PMOS transistor to the drain of the lowermost NMOS transistor, whereby the two sides are not connected to each other in the Metal i-1 position.

56 The basic transistor circuitry, as shown in Figure 10, is in a driver cell (TZ) where several of them can be connected in both the east-west and north-south directions to adjust the driver strength. If two transistor circuits (BT) of the driver cell (TZ) were connected in the north-south direction via the lines (112, 113, 114, 115) running in this direction and the switches were set to form functional inverters, the skilled person would reach the object of auxiliary claim 1 (= main claim in the appeal proceedings) in an obvious way. The fact that the fifth and sixth interconnection were not exclusively arranged in the second connection level, but also in the first interconnect level, was harmless.

57 The RF6560 chip was obviously pre-used, at least in the M1D656105 version. This had been subjected to reverse engineering, the results of which were presented in the Tech Insights report (RF6560 Analysis, June 26, 2020; K46). With regard to the further version M1D656097, construction drawings (Schematics RF6560 M1D656097; K14) had been submitted. In the area relevant for the assessment of the patent in suit, there were no relevant deviations. K46 showed that the RF 6560 chip must have been installed in at least six smartphones sold before the priority date of the patent in suit. It must have been clear to the authors of K46 that there may have been several versions of the chip and that version M1D656105 was the subject of the investigation.

58 The teardown report according to Annex K16 (ABI Research Teardown, Samsung Galaxy S II I9100 p. 28, 57) showed that the chip with the version number M1D656105 was dated April 24, 2010 and had been installed in a cell phone that had only been available from May 2, 2011. However, this does not constitute a significant contradiction, since semiconductor chips can be manufactured in stock and the indication "sample date" does not necessarily mean that the chip was removed from the smartphone on that date. It could also be the date of manufacture or the date of purchase of a chip of the same type. Even if it was unclear where the chip came from, K16 would still show that it had been available to the interested public in the version M1D656105 before the priority date.

59 Compared to the obviously pre-used chip RF 6560, only the subject matter of auxiliary claim 3b "new (= auxiliary claim 3a" in the appeal proceedings) proved to be new and based on inventive step. It had been obvious to interchange the third and fourth metallization level, i.e. to connect the drains in the third metallization level and the sources in the fourth metallization level. However, it was not obvious to connect the seventh interconnect, i.e. the connection of all drains, to an output of the device, since the seventh interconnect, which was located in the fourth metallization level during prior use, also served as a bond pad and thus as an output.

60 III. This assessment with regard to the version defended with the second-instance main claim withstands the review in the appeal proceedings as a result.

61 1) Contrary to the opinion of the Patent Court, the subject matter defended by the main request was not obvious on the basis of K9.

62 a) As also assumed by the Patent Court, the subject matter defended by the second-instance main request proves to be new compared to K9.

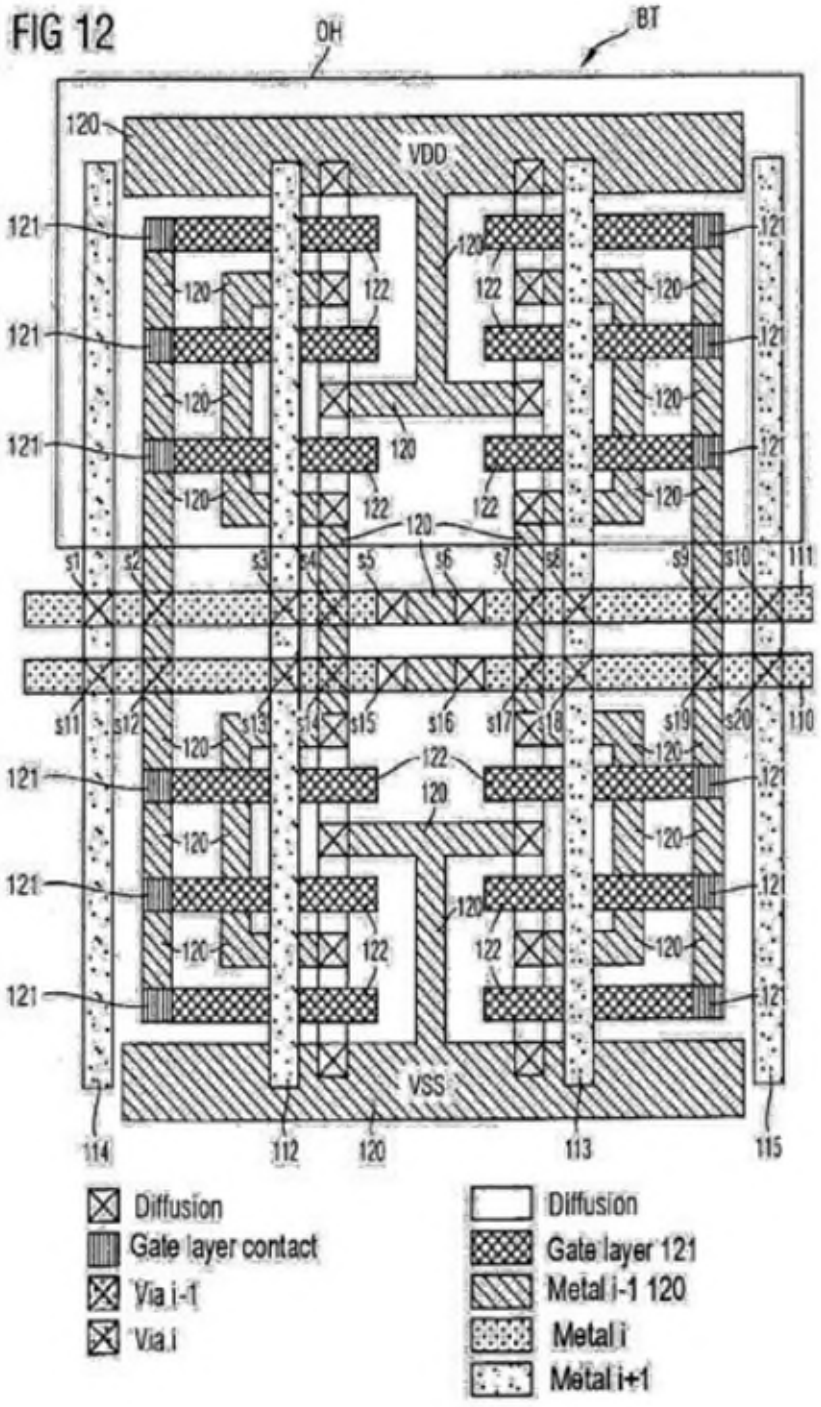
63 aa) K9 relates to the architecture of functional blocks and wiring in structured application specific integrated circuits (sASICs) and configurable driver cells of a logical cell array.

64 (1) The logic cells of such semiconductors could be formed in an active layer containing CMOS structures. The logic functions would be defined by several wiring layers arranged above the active layer and serving the wiring within a single cell (para. 3). Other wiring layers were used to provide supply voltage and to transmit and derive signals (para. 4 et seq.). In sASICs, prefabricated logic cells would be used in whole or in part, which could be combined with memory structures. Some of the wiring could be adapted to the particular application. However, from a cost point of view, as many wiring layers as possible should be permanently predefined (para. 8 et seq.). Long lines would often have to be arranged at the output of a function block. These could lead to signal delays and require refreshing of the signal (para. 14).

65 To address the resulting problems, K9 proposes a new design principle in which the functional blocks are arranged in a regular array formed in an active layer and at least a first wiring layer. A corresponding array of wiring layers is provided for routing signals. This comprises at least two wiring layers with non-parallel lines and an insulation layer in between. At least in one layer the

lines are designed as segments which are continuous within a wiring field and interrupted at the boundaries of the wiring fields (para. 20).

66 (2) Figure 12 reproduced below shows an example of a base transistor structure consisting of two identical substructures located side by side and formed by lines (120) in the i-1-th wiring layer.

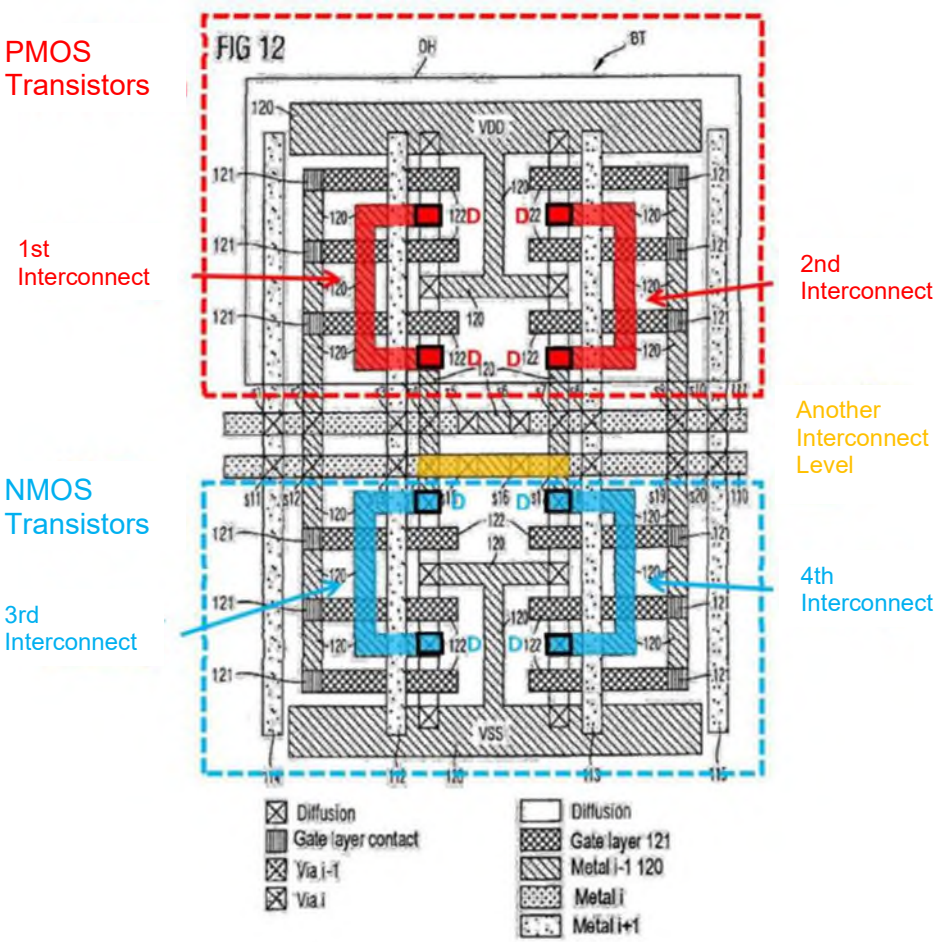


67 Each substructure has three transistor gates of stripe transistors in its upper and lower halves. The transistor gates are located where the gate layer (122)

overlaps the diffusion regions. This is a parallel circuit of three inverters formed by connecting the transistors in parallel (para. 99).

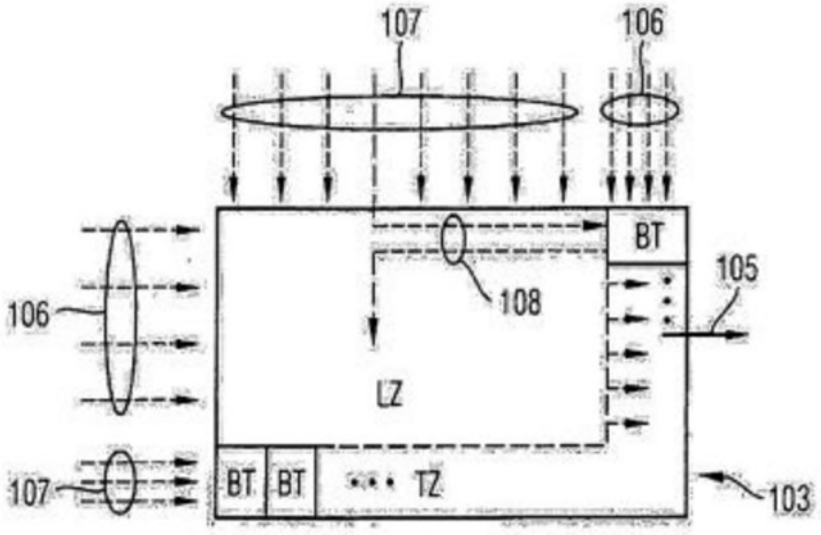
68 The base transistor structure is contacted by two wiring lines (110, 111) located in the metallization layer i and running in the west-east direction and four wiring lines (112 to 115) located in the metallization layer i+1 and running in the north-south direction and can be configured with regard to its driver strength. Additional wiring lines in layer i+1 without predefined configuration options with respect to the driver block are possible in the free spaces (para. 98). The switches s1 to s20 are mask programmable (para. 100).

69 According to the findings of the Patent Court, the gates and sources are connected to the potentials VDD or VSS in the first layer Metal i-1 (120). For the drains, there is one connection each on the left and right sides, each extending from the drain of the uppermost PMOS transistor to the drain of the lowermost NMOS transistor. The two sides are not connected in the Metal i-1 (120) layer. By setting the switches appropriately, a connection can be made in the Metal i layer via switches s4 and s7 and a piece of wire in the Metal i-1 (120) layer and switches s5 and s6. A corresponding connection can be made through switches s14, s15, s16, and s17, as shown in the following figure, which has been supplemented by the applicant. Both connection possibilities are explicitly disclosed as a possibility in K9 (para. 105).



70 (3) Figure 10 reproduced below shows the arrangement of a plurality of base transistor structures (BT) in an L-shaped driver cell (TZ). The driver strength can be influenced by suitable contacting of base transistor structures (para. 92). Together with a logic cell (LZ), the driver cell (TZ) forms a logic block of the ASIC.

FIG 10



71 bb) Thus, as the defendant also does not dispute in the appeal proceedings, features 1 to 1.9 are disclosed.

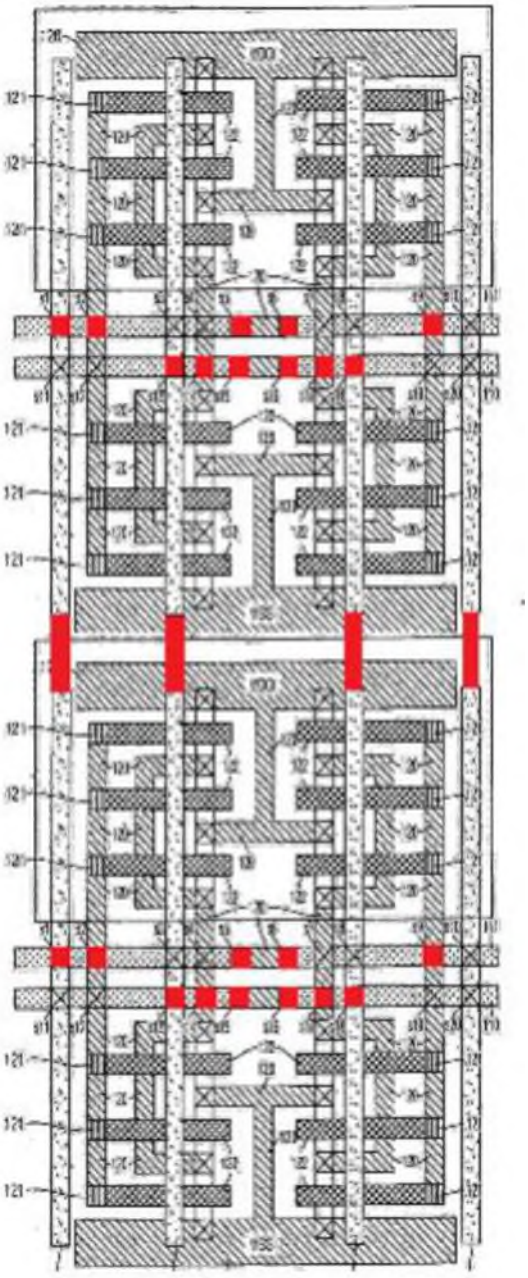
72 cc) Not disclosed is the entirety of features 1.11 to 1.13.

73 As the Patent Court correctly pointed out in the reference granted under Sec. 83 (1) Patent Act, a connection via switches s4, s5, s3, s13, s15 and s14 as well as switches s7, s6, s8, s18, s16 and s17 would indeed realize the features mentioned when viewed in isolation. However, as the defendant has explained in detail and as the Patent Court did not question, this would not result in a functional circuit, because the gates and the drains would then also be interconnected.

74 The connection explicitly mentioned in K9 via switches s4, s5, s6 and s7 or s14, s15, s16 and s17 is also not sufficient. In this embodiment, part of the connection is on the first connection level. This contradicts the specification from features 1.5 and 1.8.

75 b) The subject matter defended by the main request was not suggested on the basis of K9.

76 Contrary to the view of the Patent Court, substituting two structures, as schematically shown in the combination of two copies of Figure 12 reproduced below, does not lead to an embodiment according to features 1.5, 1.8 and 1.11 to 1.13.



77 In this embodiment, the interconnects for the drains on the left side are interconnected with those on the right side in both substructures via switches s14, s15, s16 and s17, respectively, which can be regarded as the fifth and sixth partial connections in the sense of features 1.11 and 1.12. These two partial connections are in turn connected to each other via the section between the two switches s13 and the two switches s18 on the two partial structures, which can be regarded as the seventh partial connection in the sense of feature 1.13.

78 In this embodiment, too, however, the connection between switches s15 and s16 runs in layer Metal i-1 (120) and thus in the first connection level within the meaning of the patent in suit. This contradicts the specification from features 1.5 and 1.8 as well as 1.11 to 1.13.

79 2. However, the Patent Court was correct in considering the RF6560 type chip as lacking novelty.

80 a) The Patent Court's finding of obvious prior use of the RF6560 chip in the M1D656105 version withstands defendants' attacks.

81 Pursuant to Sec. 117 (1) Patent Act and Sec. 529 (1) No. 1 Code of Civil Procedure, the facts established in the first instance are to be used as a basis in the appeal instance, unless specific indications give rise to doubts as to the correctness or completeness of the findings relevant to the decision and therefore require a renewed determination.

82 Such indications are neither shown nor otherwise evident in the case in dispute.

83 aa) The Patent Court based its assessment on a teardown report by the company Tech Insights (RF6560 Analysis, June 26, 2020; K46), on a teardown report by the company ABI research (Samsung Galaxy S II I9100 Teardown, K16)

and on digital design drawings by the supplier Quorvo (K14).

84 In K46, excerpts from a database maintained by Tech Insights schematically show that this company found a chip with the type designation RF6560 and the version number M1D656105 in six different cell phone models made by Samsung, LG, and Meizu that were purchased between July 13, 2011 and July 17, 2002 (p. 2).

85 The phone models listed in K46 include the Samsung Galaxy S II I9100, which also according to the information in K16 contained a chip with the type designation RF6550 and the version number M1D656105. Photos are included in K16 and K46, according to which the mentioned version number and the year 2010 are indicated on the chip.

86 K46 also shows details of the structure of the chip. According to the findings of the Patent Court, the structure of the chip is identical to the structure of the chip described in K14 with the same type number and the different version number M1D656097 with regard to all features relevant to the dispute.

87 bb) In this initial situation, the Patent Court was allowed to come to the conclusion in its assessment of the facts that the information in K46 is correct in content, although the defendant did not dispute this with knowledge and pointed out circumstances that could lead to a different assessment. The objections already raised by the defendant in the first instance and repeated in the appeal do not show any concrete indications that give rise to doubts about the correctness or completeness of the findings made.

88 (1) Contrary to the view of the defendant, K46 is not to be regarded as unsuitable evidence because the information contained therein on types, version numbers and purchase dates originates from a database maintained by Tech Insights itself and the content of the folder structure shown and its connection to the

information is only presented in an overview and is not explained in detail.

89 The circumstance described may theoretically give rise to the risk that individual or all statements are inaccurate or incomplete. Whether this risk gives rise to practically relevant doubts about the truth of the claim put forward by the plaintiff in evidence is, however, a question for the assessment of the facts by the court.

90 The Patent Court considered the information in question to be sufficiently reliable because it is detailed and consistent in itself and because it granted Tech Insights sufficient expertise to identify any inconsistencies. This assessment stands up to scrutiny against the above-mentioned standard.

91 (2) The Patent Court was not correct in disregarding K16 and K46 because, according to the copyright notices contained therein, both reports were prepared after the priority date, namely in 2018 and 2020, respectively.

92 According to the plaintiffs' submission, K16 and K46 do not constitute prior art citations. Rather, they serve as documentary evidence that the chip with the type designation RF6560 and the version number ...105 was publicly available before the priority date. In this respect, they constitute suitable evidence.

93 Whether the information contained in K16 and K46 is correct in terms of content is a question of evaluating the evidence. For this, the relatively late date of preparation can also be of importance.

94 The Patent Court also took this circumstance into account. Its conclusion that the information in K16 and K46 reliably reflects the prior art is not subject to any serious doubts in this respect either.

95 (3) There are also no concrete indications for doubts about the correctness and completeness of the findings made because K46 and K16 show a different version number than K14.

96 The Patent Court took this deviation into account and, with unobjectionable considerations, considered it irrelevant for the assessment, because the two versions correspond in the features relevant for the dispute and because the version indications in K46 and K16 correspond.

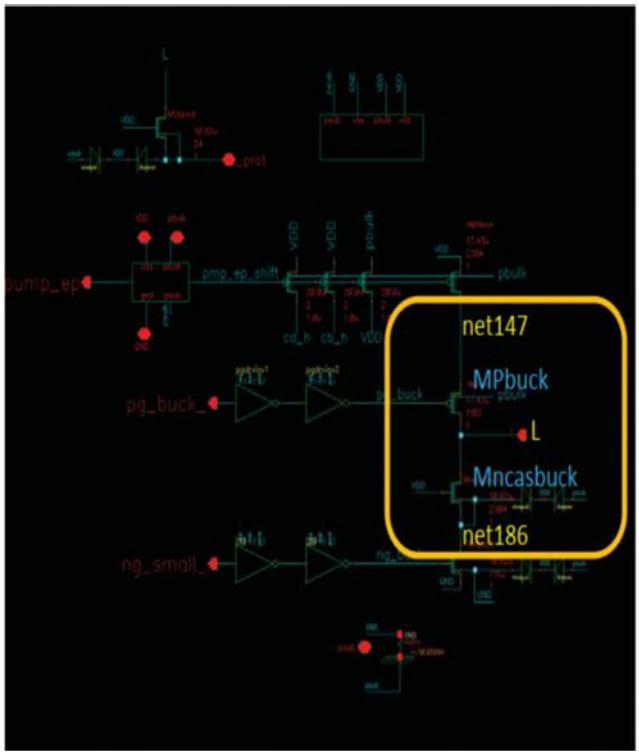
97 (4) The fact that K16 contains the indication "Sample date 4/24/2010" with regard to chip RF6560 does not lead to a different assessment.

98 The Patent Court also took this circumstance into account. In particular, it saw that the said indication could give rise to doubts if it referred to the date on which the cell phone under examination was purchased because, according to plaintiff's submissions, cell phones of the type under examination were only available from May 2, 2011. It nevertheless considered the indication to be plausible because it can also refer to the date of manufacture of the chip. This consideration is convincing, especially since, as shown by the photos reproduced in K46 and K16, the year 2010 is indicated on the outside of the chip.

99 Against this background, the conclusion drawn by the Patent Court that K46 would have evidentiary value even if the specifically examined chip did not originate from a cell phone of the specified type, but rather, on the basis of the version number found, the data of another chip of this version examined earlier was used, is also not objectionable.

100 b) The chips shown in K14 and K46 anticipate all features of the subject matter defended by the main request.

101 aa) The chip shown in K14 with the version number ...097 has NFET and PFET areas with the interconnection shown below (p. 4).



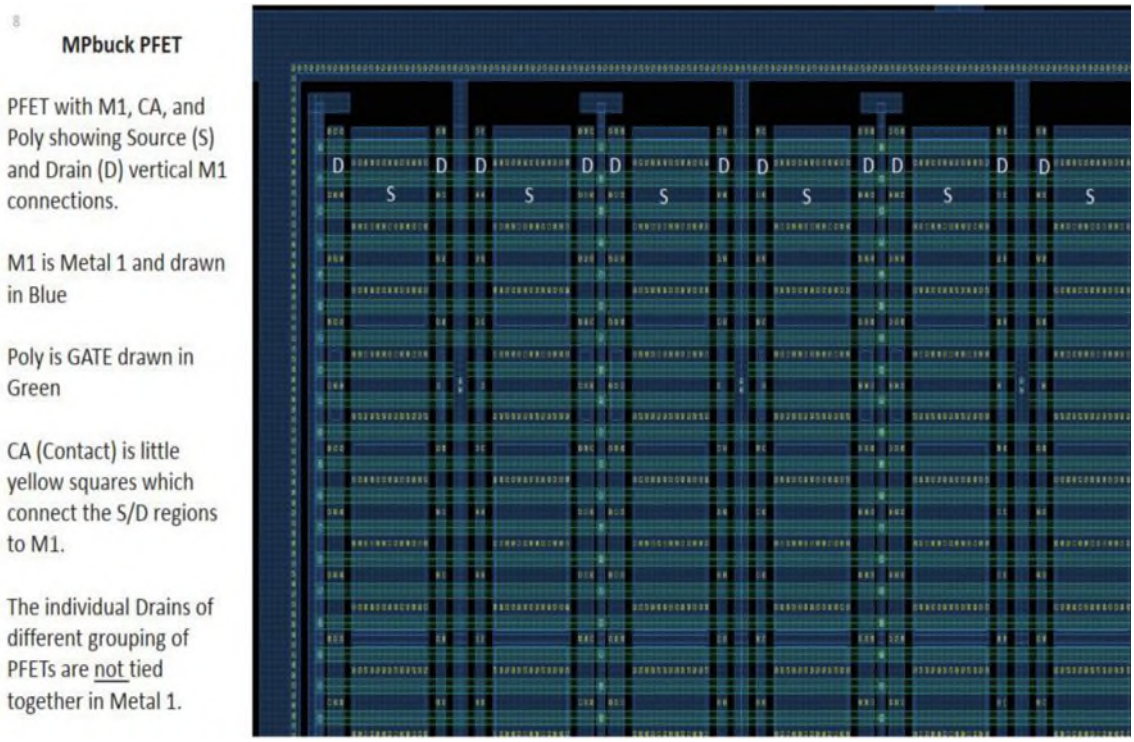
MPbuck is a PFET whose Source is tied to net147, and Drain is tied to node "L".

Mncasbuck is an NFET whose Source is tied to net186, and Drain is tied to node "L".

These are power FETs whose drains are tied together.

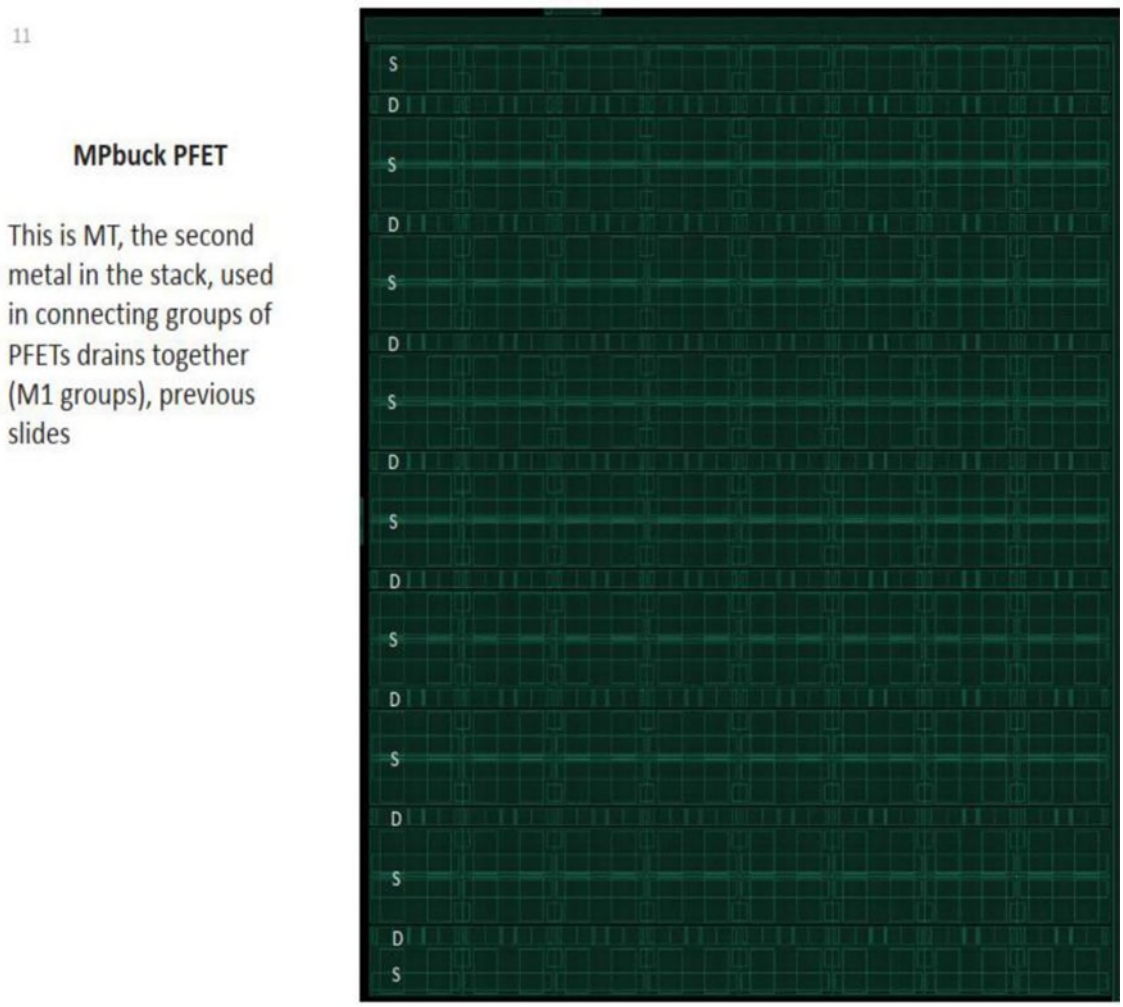
102 bb) According to the findings of the Patent Court, the structure of the chip with the version number ...105 shown in K46 is identical to that shown in K14 in the area relevant here and shown below.

103 As can be seen, among other things, from the photograph reproduced below on page 8, the PMOS transistors are located in a large number of vertical lines on a first metallization level M1 (blue) with polysilicon gates (green) running from left to right. The gates, sources (S) and drains (D) are contacted by the vias drawn in yellow.



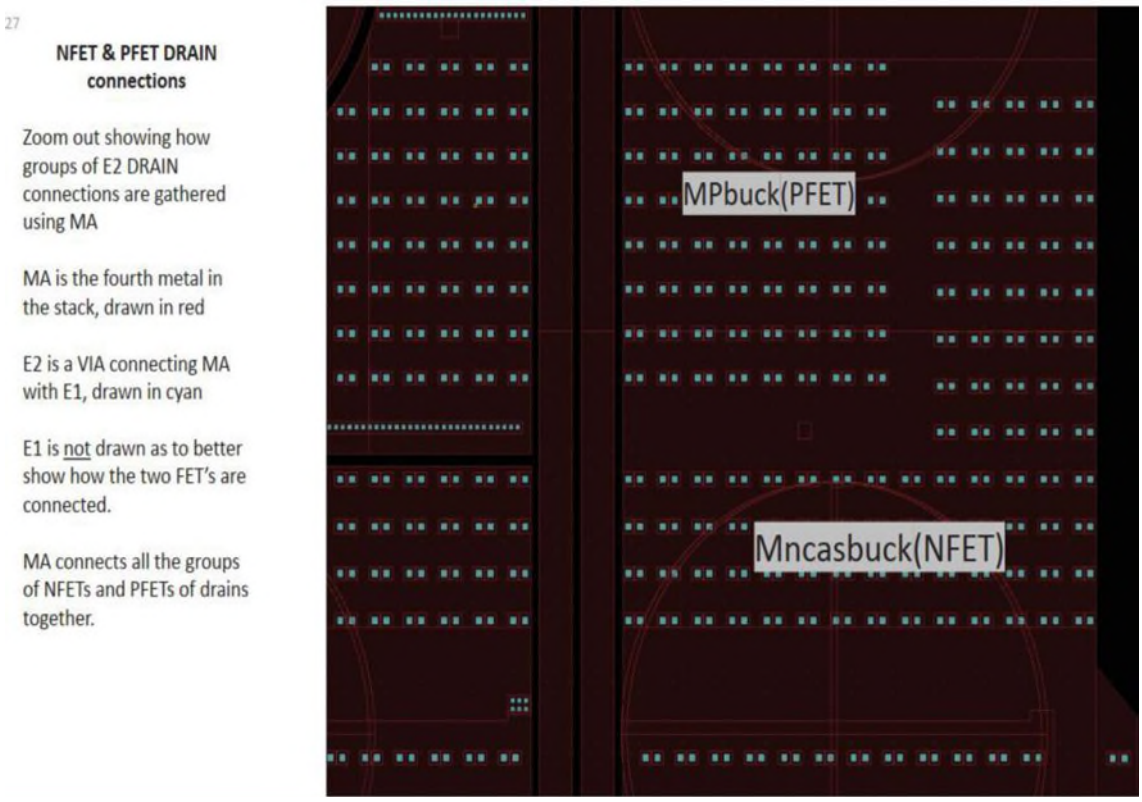
104 In the area marked D, the drains on the metallization level M1 are connected by strips running from top to bottom. At least behind the fourth strip marked D, counted from the left, there is no connection to the drain strips running in front of it.

105 The photograph on page 11 reproduced below shows a second metallization level MT through which drains of the plurality of PMOS transistors are interconnected by means of metal strips running from left to right.



106 The NMOS transistors are arranged in a corresponding manner.

107 After a further level E1 (p. 22), the drains of the PMOS and NMOS transistors are connected in a fourth metallization level MA, as shown in the photograph on page 27 reproduced below.



108 cc) Thus, as the defendant also does not doubt, features 1.1 to 1.13.1 are disclosed.

109 dd) Contrary to the view of the defendant, the disclosed semiconductor is a CMOS device according to feature 1.

110 As already shown above, it is sufficient for this that the semiconductor was manufactured in CMOS technology. Whether it also contains CMOS logic is irrelevant.

111 IV. With regard to the auxiliary requests 1 and 1a as well as the variants marked with one and two apostrophes, respectively, there is no deviating assessment.

112 1. The variants provided for all applications, marked with an apostrophe, in which feature 1.13.1 is omitted, is not to be assessed differently with regard to patentability, if only because this feature is optional according to the main request.

113 2. For the variant marked with two apostrophes, which provides for feature 1.13.1 as a mandatory feature, there is also no different assessment.

114 This feature is also disclosed by prior use RF6560.

115 (a) According to modified feature 1.13.1, the output of the device shall be connected to the seventh interconnect.

116 It is true that this does not specifically indicate the manner in which the connection is to be made. However, as the Patent Court correctly pointed out in connection with the upheld version which it considered to be legally valid, it follows from the context of the specifications contained in claim 1 regarding the different interconnects and connection levels that the exit must be assigned to the seventh interconnect in spatial-physical terms and may not be configured in such a way that it can be assigned to another connection at the same time.

117 This rules out the possibility that the connection is merely mediated via another interconnect or connection level.

118 b) The Patent Court rightly decided that this embodiment is disclosed by prior use RF6560.

119 In the arrangement shown in K46, the seventh interconnect located in the fourth metallization level (p. 3 and 6 each on the right) serves as a bond pad and thus as an output for the chip. This corresponds to the specifications shown above.

120 3. The cancellation of feature 1.9 provided for under auxiliary request 1 does not lead to a different assessment either.

121 As already explained above, it does not follow from feature 1.9, contrary to the opinion of the Patent Court, that the fifth and sixth interconnects may partially run in the first interconnect level. The cancellation of this feature does not lead to a substantive change of the protected subject matter in this respect.

122 4. The addition to auxiliary claim 1 provided for in auxiliary claim 1a to the effect that the first and second interconnects may not be connected to the third or fourth interconnect on the interconnect level precludes embodiments such as those shown in Figures 9 and 11.

123 This limitation cannot lead to the affirmation of inventive step, because it is not recognizable which advantages it brings in comparison to the solution according to the model of figure 11, which is already disclosed in the prior art and presented as particularly advantageous in the patent in suit.

124 V. The subject-matter defended by auxiliary claim 2a, on the other hand, is patentable.

125 1. According to auxiliary request 2a, which corresponds to the first-instance auxiliary request 1b, claim 1 should be amended as follows in the version of the second-instance main request:

- the following feature 1.22 should be inserted before feature 1.3:

> at least three metal layers above the drains of the transistors, comprising a first metal layer, a second metal layer and a third metal layer; wherein the first metal layer is the lowest metal layer above the drains, the second metal layer is the next metal layer above the first metal layer and the third metal layer is the next metal layer above the second metal layer;

- in feature 1.3, the words "on an interconnect level" should be replaced by "on a first interconnect level on the first metal layer";

- in the features 1.4, 1.5, 1.6, 1.7 and 1.8, the word "first" should be inserted before the word "inter-connect level";

- in feature 1.11, after the words "on a second interconnect level" to insert: "on the second metal layer";

- in feature 1.13, after the words "on a third interconnect level" to insert: "on the third metal layer".

126 2. The resulting changes require further consideration.

127 a) Contrary to plaintiff's view, no further metal layers may be arranged between the three metal layers provided for in feature 1.22.

128 This follows from the specification in feature 1.22 that the second and third metal layers are each the next metal layer above the first and second layers, respectively.

129 b) From the synopsis with the modified features 1.3, 1.11 and 1.13, it can be seen that the three interconnect levels provided thereafter are arranged in the three metal layers according to feature 1.22.

130 This results from the reference to "the" metal layer with the corresponding ordinal number in all three features mentioned at the beginning.

131 3. Contrary to plaintiff’s view, feature 1.22 is disclosed in the originally filed documents as belonging to the invention.

132 a) Like the patent specification, the application - the contents of which correspond to the document of disclosure (K3) - in connection with the embodiments according to Figures 2 and 3 speaks only of "one" or "the" first, second and third metal layers, without specifying their position more precisely (paras. 36-38). In contrast, in connection with the embodiment according to Figures 4 to 13, the layers are referred to as M1, M2 and M3 (paras. 39-61).

133 aa) The designations M1, M2 and M3 are commonly used for the lowest three layers on a chip, according to the Patent Court's findings regarding feature 1.21 provided for in some of the auxiliary requests at first instance. Thus, as the Patent Court also correctly assumed, the arrangement provided for in feature 1.22 is originally disclosed.

134 bb) To the extent that the plaintiff, on the other hand, wants to understand the abovementioned designations as mere ordinal numbers, it does not show any circumstances which could indicate that the designations are used in the application in deviation from the usual linguistic usage.

135 In the embodiments, the three layers immediately follow each other and a layer arranged below the layer M1 is not mentioned.

136 It cannot be inferred from the fact that Figures 4 to 13 show a highly schematized representation focused on the connection of the drains that the designations M1, M2 and M3 used in this context are used in a meaning that deviates from the usual technical usage. It is true that it follows from the context that the device described must also contain connections for other elements, in particular for sources and gates. However, even according to plaintiff's submission, this does not necessarily require that additional layers be inserted between or under the layers shown in the embodiments.

137 Whether the designation M1 is used in a different sense in European patent application 2 378 806 (K6) or in US patent 7 112 855 (K54) does not require a final decision. Even if this were to be affirmed, there would be no concrete indications that the application for the patent in suit is also based on an understanding that deviates from the usual technical usage.

138 b) Against this background, it can be left open whether the application also discloses deviating embodiments as belonging to the invention, in which additional layers serving other purposes are arranged between or below the three layers used for connecting the drains. Even if this were to be affirmed, it follows from the description of the above-mentioned embodiments that in any case also such embodiments are claimed in which additional layers are not present at the places mentioned.

139 c) Contrary to plaintiff's view, it cannot be inferred from the application that the device may only have three metal layers.

140 The application and the patent in suit deal with only three layers. However, it is sufficiently clear from the fact that other elements of the device must be connected to each other in addition to the drains, which are the focus of the consideration, and that the application does not specify this, that further layers may be present.

141 4. The subject matter defended by auxiliary claim 2a is patentable.

142 (a) By K9, this subject matter was not disclosed or suggested for the same reasons as the subject matter defended by the second-instance main request.

143 b) By prior use RF6560, said subject matter was also neither disclosed nor suggested.

144 aa) As the Patent Court correctly pointed out in connection with the first instance auxiliary request 3b, the modified feature 1.13 is not disclosed in K14 and K46.

145 The connections between the fifth and sixth interconnects are only passed through the third metallization level in K14 and K46 and are not made until the fourth metallization level (K14 p.13 et seq. and p. 22 et seq.).

146 bb) Contrary to the opinion of the Patent Court, the modified feature 1.13 was not obvious on the basis of the prior use RF6560.

147 (1) According to the findings of the Patent Court, it is basically irrelevant from a technical point of view in which order the two metallization levels are arranged to connect the drains and the sources.

148 However, according to the defendant's submission, which remained uncontradicted in this respect, it was not possible without further ado to use the third metallization level used for the connection of the sources for the connection of the drains instead, based on the setup shown in K14 and K46, because then the connection by means of bond pads shown in K14 and K46 would not be possible in the fourth level, which would make a further reconfiguration necessary.

149 Against this background, it required a special suggestion to exchange the function of the third and the fourth metallization level. As the Patent Court correctly pointed out in connection with the version it considered to be legally valid, such a suggestion did not result from K14 or K46 or from other circumstances.

150 (2) The fact that K14 shows a connection for the drains in the third metallization level in another place, which was additionally used by the Patent Court, does not speak against, but also in favor of the affirmation of inventive step.

151 The different order of the source and drain connections at different locations on the chip also suggests that the choice between the possibilities under consideration is not arbitrary but is based on other circumstances of the configuration. Also under this aspect, it required a special suggestion to change the order revealed in K14 and K46 in the area relevant here.

152 VI. The decision on costs follows from Sec. 121 (2) Patent Law and Sec. 97 (1) and Sec. 92 (1) sentence 1 ZPO.

Bacher Hoffmann Deichfuß

Marx Crummenerl

Lower court:
Federal Patent Court, Decision of October 22, 2020 - 2 Ni 21/20 (EP) -