Machine translation

FEDERAL SUPREME COURT

ON BEHALF OF THE PEOPLE

JUDGMENT

X ZR 26/21

Announced on:
March 16, 2023
Schönthal
Clerk of the Court
as Clerk of the
Registry

in the patent nullity case

ECLI:EN:BGH:2023:160323UXZR26.21.0

The X. Civil Senate of the Federal Supreme Court, at the oral hearing on March 16, 2023, by Dr. Deichfuß and Hoffmann, Judges Dr. Marx and Dr. Rombach, and Judge Dr. Crummenerl

found to be right:

The appeal against the judgment of the 5th Senate (Nullity Senate) of the Federal Patent Court of December 9, 2020 is dismissed.

The costs of the appeal proceedings shall be borne by the plaintiff 1.

By law

Facts:

1 The defendant is the owner of European patent 2 460 270 (patent in suit), which was granted with effect for the Federal Republic of Germany, was filed on July 28, 2010, claiming two U.S. priorities dated July 28 and November 20, 2009, and concerns a switch.

2 Claim 1, to which further ten claims are referred back, reads in procedural language:

> An apparatus comprising
> a plurality of transistors (510) coupled in a stacked configuration and arranged to receive an input signal and to provide an output signal; a plurality of resistors (520) coupled to gates of the plurality of transistors; and an additional resistor (530) coupled to the plurality of resistors and arranged to receive a control signal for the plurality of transistors characterized in that the apparatus further comprises:
> a second plurality of resistors (540 a-k) coupled to bulk nodes of the plurality of transistors; and a second additional resistor (540) coupled to the second plurality of resistors and a bulk voltage.

3 Claim 12, to which three further claims are referred back, protects a device comprising a module with a plurality of switches, each of which comprises a device according to claim 1. Finally, claim 16, to which two further claims are referred back, protects a method for switching a signal with a device according to claim 1.

4 The plaintiffs have argued that the subject matter of the patent in suit is not patentable. The defendant has defended the patent in suit as granted.

5 The Patent Court dismissed the complaint. Plaintiff 1 contests this with its appeal, in which it continues to seek a complete declaration of nullity of the patent in suit. The defendant opposes the appeal.

Reasons for Decision:

6 The admissible appeal of plaintiff 1 is unsuccessful.

7 I. The patent in suit relates to a switch having a plurality of transistors coupled and arranged in a stacked configuration.

8 According to the description of the patent in suit, such a switch can receive an input signal at a source or drain terminal and a control signal at a gate terminal. If the switch is switched on by the control signal, the input signal is passed on to another source or drain terminal. If the switch is turned off, the signal is blocked (par. 2).

9 The performance of such a switch could be affected by parasitic capacitances. As the patent in suit explains, using the example of a switch with an NMOS transistor shown schematically in Figure 3A, this can result in a portion of the input signal V_{IN} passing through a leakage path via a parasitic gate-to-source capacitance (C_{GS}) and a parasitic gate-to-drain capacitance (C_{GD}) when the transistor is on (paragraph 19).

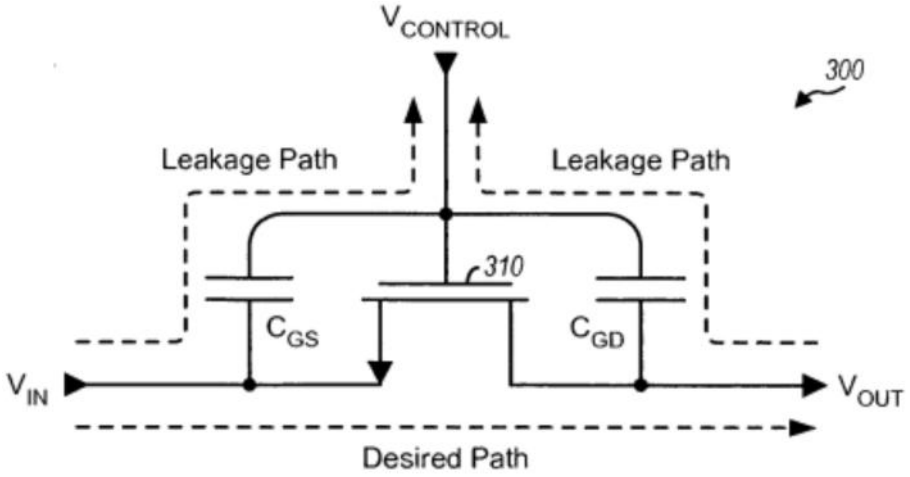

FIG. 3A

10 Especially in high-frequency applications, the resulting signal loss can be considerable (par. 19). This can be countered by inserting a resistor (R) with a high resistance value, for example in the kΩ range, between the gate terminal of the transistor and the source of the control signal. This could turn the gate of the transistor into a so-called floating gate and reduce the signal loss considerably. The resistor R could be called an RF floating resistor (par. 20).

11 An example of such an arrangement is shown in Figure 3B.

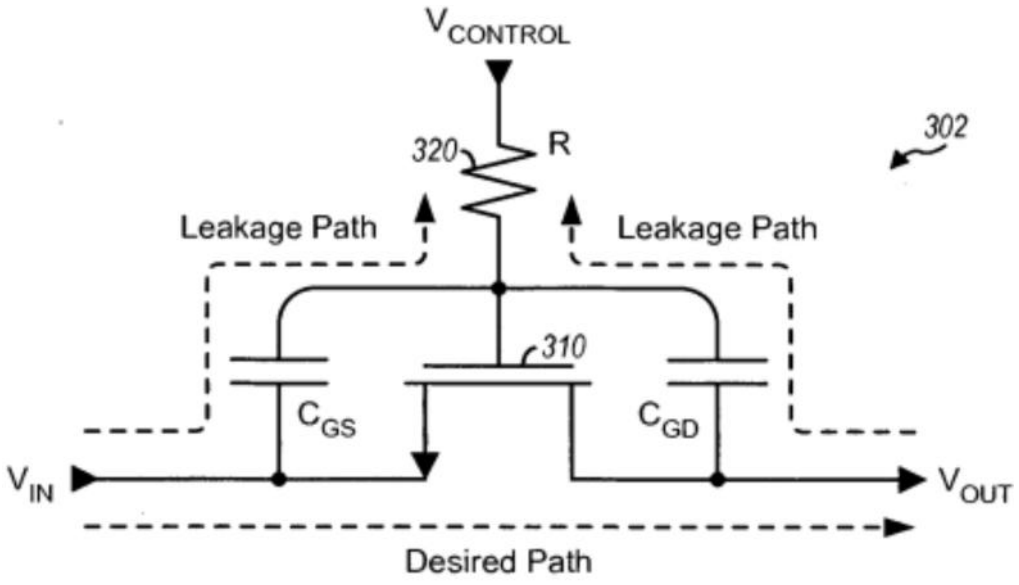

FIG. 3B

12 Furthermore, the reliability of a transistor could be affected by the fact that when the transistor is off, the gate-to-source voltage (V_{GS}), which depends on the signal swing of the V_{IN}-signal, exceeds the breakdown voltage of the transistor (par. 21). This could be countered by a stacked arrangement of several transistors. An example of such an arrangement is shown in Figure 4.

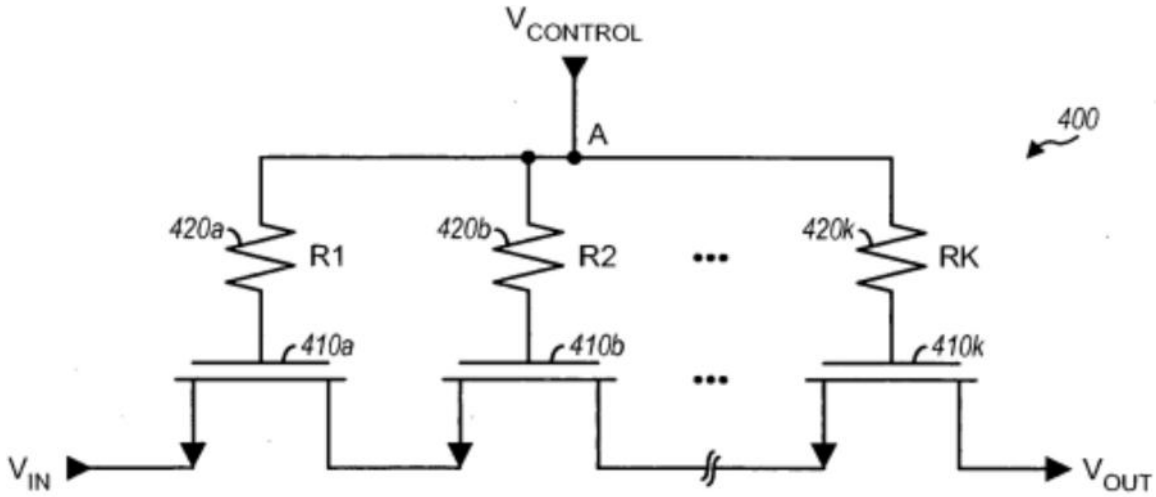

FIG. 4

13 Here, multiple transistors 410a through 410k are coupled in a stacked configuration, where K is an integer >1. For each transistor - except the first and the last - the source is coupled to the drain of the previous transistor.

14 Further, a corresponding number of resistors 420a to 420k are provided, each connected to the gate of a transistor and a node A to which the control signal $V_{CONTROL}$ is applied (par. 22).

15 When the transistors are on, resistors 420a through k can reduce signal loss due to parasitic capacitances, as discussed above, by providing a large resistance to the V_{IN}-signal in the leakage path through the C_{GS} and C_{DS} capacitances (par. 23).

16 With the transistors off, resistors 420a through k can help distribute the voltage swing of the V_{IN}-signal evenly across the stacked transistors (par. 23).

17 As the patent in suit explains, there may be further advantages in providing an additional resistor between node A and the source of the control signal (paras. 27-29). A corresponding arrangement is shown in Figure 5.

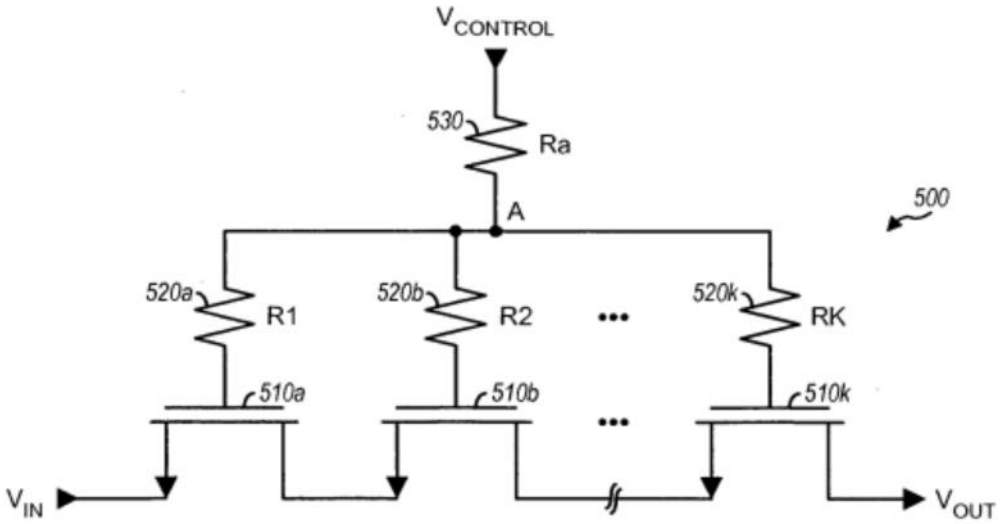

FIG. 5

18 Resistor 530 is designated as an additional RF floating resistor (par. 27, par. 29).

19 Switches with improved reliability could also be implemented with P-channel MOS (PMOS) transistors, complementary metal oxide semiconductor (CMOS) transistors, junction transistors (BJTs), bipolar CMOS (BiCMOS) transistors, silicon-germanium (SiGe) transistors, gallium arsenide (GaAs) transistors, etc. (para. 31).

20 2. Against this background, the technical problem can be seen in improving the reliability of a switch using transistors with four externally switchable terminals.

21 3. To solve this problem, claim 1 provides a device whose features can be divided as follows:

22

1.	An apparatus comprising	Eine Vorrichtung, umfassend
1.1	a plurality of transistors (510) coupled in a stacked configuration and arranged to receive an input signal and to provide an output signal;	eine Vielzahl von Transistoren, die in einer gestapelten Konfiguration gekoppelt und angeordnet sind, um ein Eingangssignal zu empfangen und ein Ausgangssignal bereitzustellen;
1.2	a plurality of resistors (520) coupled to gates of the plurality of transistors; and	eine Vielzahl von Widerständen, die mit Gates der Vielzahl von Transistoren gekoppelt sind, und
1.3	an additional resistor (530) coupled to the plurality of resistors and arranged to receive a control signal for the plurality of transistors	einen zusätzlichen Widerstand, der mit der Vielzahl von Widerständen gekoppelt und angeordnet ist, um ein Steuersignal für die Vielzahl von Transistoren zu empfangen
1.4	a second plurality of resistors (540 a-k) coupled to bulk nodes of the plurality of transistors and [1.4 und 1.4.1]	eine zweite Vielzahl von Widerständen, die mit Bulk-Knoten der Vielzahl von Transistoren gekoppelt sind und
1.5	a second additional resistor (540, [richtig: 550]) coupled to the second plurality of resistors and a bulk voltage [1.4.2]	ein zweiter zusätzlicher Widerstand, der mit der zweiten Vielzahl von Widerständen und einer Bulk-Spannung gekoppelt ist

23 Such an arrangement is shown by way of example in Figure 6 of the patent specification in dispute, in which the reference sign for the additional resistor on the bulk side must correctly read 550 (instead of 540).

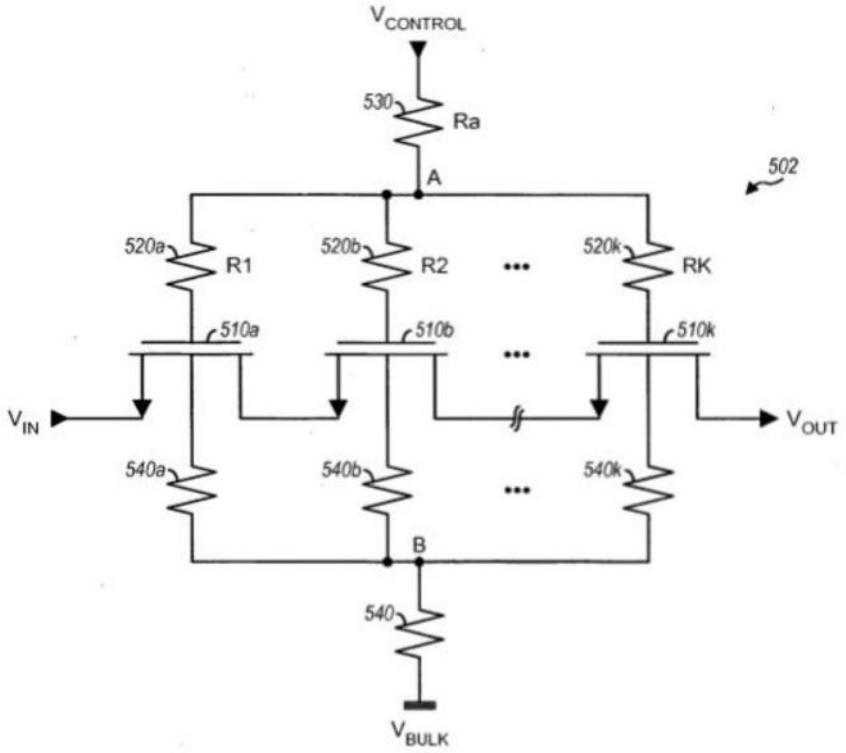

FIG. 6

24 Here, the switch comprises k resistors 540a to 540k, each arranged between the bulk node of transistors 510a to 510k and bulk node B. An additional resistor 550 is disposed between the node B and the source of the bulk voltage V_{BULK}. Resistors 540 (a-k) and 550 provide RF floating of the bulk node of transistors 510 (a-k), which, according to the disclosure in the patent in suit, has similar advantages to those obtained with resistors 520 (a-k) and 530 on the gate side (para. 30).

25 Claim 12 relates to a device in which a plurality of switches according to claim 1 are used, claim 16 relates to a method for signal switching with a device according to claim 1. The objects of these claims are thus characterized by the same features as patent claim 1 and are subject to the same assessment.

26 4. The figures of the patent in suit refer to NMOS transistors. However, the claim is not limited to this type of transistors. It follows from feature 1.4 that the transistors must have four externally switchable terminals (source, drain, gate and bulk).

27 Claim 1 does not specify the type of input and output signal. According to the description, these can be high-frequency signals.

28 Also with regard to the value of the bulk voltage and the various resistors or their relationship to each other, no specifications can be taken from claim 1.

29 II. The Patent Court gave the following main reasons for its decision:

30 The subject matter of claim 1 is patentable. It is not anticipated by the paper "Design and Analysis of Transmit/Receive Switch in Triple-Well CMOS for MIMO Wireless Systems" (Poh/Zhang, IEEE Transactions on Microwave Theory, 2007, pp. 458-466, NKD1). NKD1 disclosed a switch with a plurality of CMOS transistors with four external terminals. Resistors were provided at both the gate and bulk terminals. These would be individual resistors in each case. An additional resistor connected to the plurality of resistors on the gate or bulk side is not shown in NKD1.

31 The subject-matter of claim 1 had not been obvious to the skilled person, a graduate engineer with a university degree in electrical engineering and with a focus on circuit technology, who had several years of practical experience in the development of semiconductor chips, on the basis of the US application 2004/0051395 (NKEP1). NKEP1 discloses a switch with a plurality of transistors.

These are field-effect transistors (FE transistors) which have three switchable terminals but no bulk terminal. A resistor order with a series connection of a plurality of resistors and an additional resistor was provided at the gate terminals of the transistors. Features 1.4 and 1.5 were not disclosed thereafter.

32 Since it was known to the skilled person that the problem of leakage currents addressed in NKEP1 does not occur with CMOS transistors with four terminals, he had reason to use transistors which in addition have a bulk terminal instead of transistors which have only three terminals.

33 However, NKEP1 does not give any suggestion as to how these connections are to be wired. Also the reference book "Halbleiter-Schaltungstechnik" (Tietze/Schenk, 12th edition 2002, NK7) does not give any hints in this respect. The person skilled in the art would also not provide the same arrangement for the bulk terminals as for the gate terminals without further ado, because he was aware that in the case of CMOS transistors with four external terminals, the gate side and the bulk side had a different structure. NKD1 also made no suggestion in this direction. This document shows that the individual resistors on the gate and the bulk side have different effects. NKD1 also did not mention an additional, common resistor. The person skilled in the art would not consider such a resistor because he knew that leakage currents did not play a role in CMOS transistors and that an additional resistor would not provide any additional benefit. There is no further suggestion from the paper "A High Power CMOS Switch Using Substrate Body Switching in Multistack Structure" (Ahn et al.; IEEE Microwave and Wireless Components Letter 2007, pp. 682-684, NKD2). There, individual resistors are provided on the bulk side, which can be short-circuited specifically for a single

transistor via a switch. This would not be possible if an additional resistor were provided. The state of the art presented further also did not provide any corresponding suggestion.

34 III. This assessment stands up to review on appeal.

35 1. The subject matter of claim 1 is new, as the appeal does not dispute. It is neither completely anticipated by NKD1 nor by NKEP1.

36 a) NKD1 is concerned with the design and analysis of a radio frequency transmit/receive switch (RF transmit/receive switch) in complementary metal oxide semiconductor (CMOS).

37 aa) Referring to Figure 3, NKD1 explains that the performance of a switch can be improved by two circuit techniques, connecting transistors in series and increasing the body resistance (p. 459).

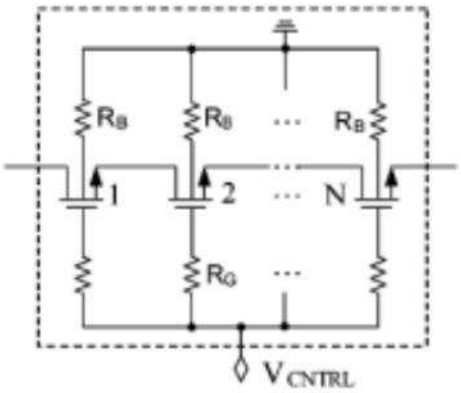

Fig. 3. Series-connected transistors for the switch.

38 The series connection of transistors serves to increase the load capacity of the switch. However, a disadvantage of this technique is that the insertion loss is considerably increased (p. 460, left column).

39 As NKD1 states, it was already known to be advantageous to provide resistors at the gate terminals (p. 460 left column). NKD1 suggests - going further - the introduction of resistors also at the body contact - called bulk node in the patent in suit. In Figure 5 of NKD1, the gate nodes and the body nodes are accordingly designated as "floating gate nodes" and "floating body nodes", respectively.

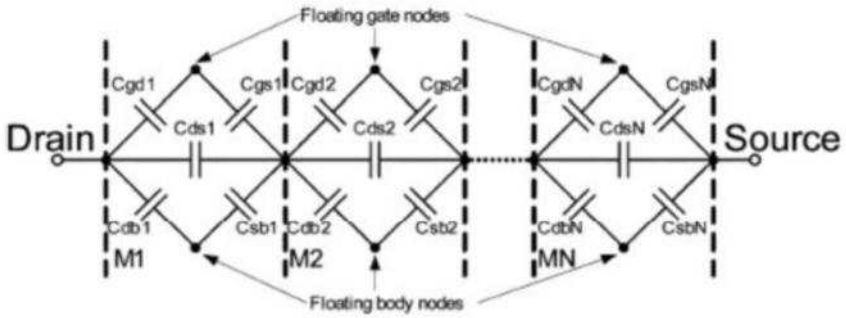

Fig. 5. Equivalent circuit of an N-series-connected transistor switch in the off state. (For the 20-finger 285-μm off-state transistor used: $Cgs = 145$ fF, $Cgd = 144$ fF, $Cdb = 2.6$ aF, $Csb = 2.8$ aF, $Cds = 15$ aF).

40 This arrangement of resistors also at the bulk terminals served not only to improve the load capacity of the switch, but also to reduce the insertion loss by reducing capacitive coupling losses through the body contact (p. 459/460). In addition, these resistors served to eliminate the coupling between the transistors, which increased the insertion loss of series-connected transistors (p. 460 left column). Figure 3 shows series-connected transistors in which the gate and body nodes are biased by using individual large resistors RG and RB (p. 460, left column).

41 The use of individual resistors is necessary to prevent signal coupling between the series-connected transistors (p. 460, left column).

42 bb) A corresponding device, shown by way of example in Figure 3, then discloses features 1, 1.1, 1.2 and 1.4.

43 cc) In contrast, feature 1.3 is not disclosed.

44 There is a lack of an additional resistor coupled to the resistors to the gate nodes to receive the control signal for the transistors coupled in a stacked configuration.

45 dd) Feature 1.5 is also not anticipated.

46 There is also no additional resistor on the bulk side, which is coupled on the one hand to the resistors at the bulk nodes of the transistors and on the other hand to a bulk voltage.

47 b) Also the US patent application 2004/0051395 ("Brindle", NKEP1) does not anticipate all features of claim 1.

48 aa) According to NKEP1, semiconductor switching devices can be realized with field-effect transistors (FETs) in which a voltage is applied to the control input. Such switches are used in particular for high-frequency signal transmission, for example radio frequency (RF) (para. 3).

49 If such a FET switch is in the ON state, it has a very low resistance which allows a signal to be conducted from the drain to the source of the FET. If a control voltage of a predetermined level (pinch-off voltage) is applied to the gate of the FET, it switches to the OFF state. It then exhibits a very high resistance that prevents a signal from flowing from the drain to the source. Such an FET switch has the advantage that the control voltage at the gate draws only little current, so that no power is consumed for the switching function (par. 4).

50 The disadvantage is that a signal which should not be conducted through the FET applies a voltage to its drain. If this voltage is greater than the control voltage, the FET switches from OFF to ON. If a low control voltage is desired, it

is therefore necessary to connect several FETs in series to divide the RF voltage. This in turn leads to an increase in the resistance of the switch in the ON state. To cope with this, it would be necessary to increase the size of the FET and thus of the chip, leading to new problems (paras. 5 to 10). This would include the switch having more leakage in the control line, which would require more power to control the switch. Thereafter, there is a need for an improved switch that can control a current output at low control voltage and provide an optimal balance of insertion loss, isolation, power handling, suppression of harmonics and leakage current in the control signal (para. 11).

51 To this end, NKEP1 proposes, among other things, a gate resistor topology that would serve to reduce the effects of leakage current flowing from the control voltage source to the gate of the FET or through the FET (para. 15, para. 61).

52 An example of such a design is shown in Figure 6c of NKEP1.

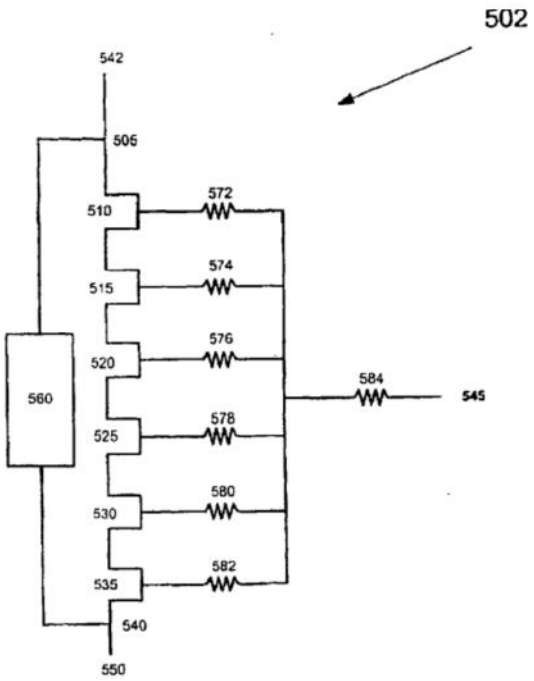

Fig. 6c

53 In this switch 502, the six series-connected transistors 510 to 535 each have first resistors 572, 574 ... 582 are provided at the gate of each of the six transistors 510 to 535 (par. 62), and a second resistor 584 is provided in series with the first resistors and coupled to the control voltage input 545 (par. 64).

54 As NKEP1 explains, the first resistors serve to reduce leakage current (par. 63).

55 Adding a second resistor increases the total resistance between the control voltage input 545 and each of the gates, thereby reducing the control current applied to the gate. Such an arrangement could be used when it is not practical or useful to increase the value of the individual resistors 572 through 582. However, it would result in an additional voltage drop process point and thus an additional leakage process point, which would reduce the process stability of the switch. The leakage current could flow through resistor 584 through any FET, since this resistor is connected to all gates. Thus, there is a trade-off between lower leakage current and process stability (par. 65).

56 bb) NKEP1 thus discloses a switch with features 1 to 1.3. However, since the field-effect transistors dealt with therein do not have a bulk connection, features 1.4 and 1.5 are not anticipated.

57 2. The Patent Court rightly decided that the subject matter of claim 1 was not suggested by the prior art at the time of priority. This applies irrespective of whether one considers NKD1 or NKEP1 as the starting point.

58 a) The subject matter of claim 1 was not obvious on the basis of NKD1.

59 aa) From this citation itself, there is no reason to provide additional, common resistors according to features 1.3 and 1.5 in addition to the plurality of resistors disclosed therein, which are coupled to the gate terminal or the bulk terminal of the plurality of transistors.

60 In any case, there is no suggestion in this regard because NKD1 emphasizes that individual large resistors are necessary to bias the gate and bulk terminals in order to prevent signal coupling between the transistors arranged in series (p. 460 left column, second paragraph). Although also NKD1 mentions that the size of a transistor is an important aspect in the design of a circuit (p. 460, left column, third paragraph) and the skilled person is aware, as also the appellant does not doubt, that the use of individual smaller resistors in combination with an additional common resistor requires less space than the use of individual large resistors, this writing thereby teaches to choose individual large resistors to avoid signal coupling between the transistors.

61 bb) NKEP1 also did not give rise to any suggestion in this direction.

62 It is true that in Figure 6c and the corresponding passage of the description, a circuit is shown in which, in addition to a plurality of resistors coupled to gates of the plurality of transistors, an additional common resistor is provided which is arranged between these individual resistors and the voltage source for the control signal. According to NKEP1, such an arrangement is suitable if the individual resistors would otherwise have to be selected too large (NKEP1 par. 65).

63 However, transferring this arrangement to the arrangement of resistors shown in NKD1 would have meant a departure from the view expressed there that individual large resistors are required to avoid signal coupling between transistors arranged in series. No general principle can be inferred from NKEP1 that individual

large resistors with a certain total resistance can be replaced by individual resistors with an additional common resistor with an identical total resistance without this having a negative influence on the signal coupling.

64 Whether the view held by the authors of NKD1 that the use of individual large resistors is necessary to prevent signal coupling between the transistors is factually correct is not decisive. The appeal does not show that it was part of the general technical knowledge at the time of priority that there are no disadvantages to be feared with regard to signal coupling if a common resistor is implemented in addition to individual resistors.

65 It can therefore be left open whether it can be inferred from NKD1 from a technical point of view that basically the same configuration can be provided for the gate and for the bulk side of transistors with regard to the arrangement of resistors.

66 In addition, the arrangement of resistors shown in Figure 6c of NKEP1 serves to prevent leakage currents from the control voltage source to the gate (see b below) and thus to overcome a problem which, according to the Patent Court's findings, does not arise with the four-terminal transistors discussed in NKD1.

67 b) The subject matter of claim 1 was not obvious even based on NKEP1.

68 aa) The switches discussed in NKEP1 contain transistors with only three terminals. Accordingly, a wiring of the bulk terminals is not discussed in NKEP1.

69 bb) The Patent Court rightly assumed that there was no reason from NKEP1 to provide the arrangement of resistors on the gate side shown in Figure

6c also on the bulk side of such a transistor.

70 As explained above, such an arrangement of resistors between gate and control voltage source is indeed advantageous because it reduces the leakage current from the control voltage source to the gate. However, according to NKEP1, it brings the disadvantage of creating an additional voltage drop point and thus an additional leakage process point. In this context, the citation explicitly speaks of a tradeoff between lower leakage current and process stability (par. 65).

71 The Patent Court has stated in this respect that it is part of the basic knowledge of the skilled person that the problem of leakage currents from the control voltage source to the gate does not arise with CMOS-based transistors having four terminals. Therefore, it is not obvious to use the resistor arrangement shown in Figure 6c of NKEP1 to avoid these leakage currents also for transistors with four terminals. A fortiori, there is then no reason to provide such a resistor arrangement also on the bulk side of such transistors.

72 The plaintiff's reference that the skilled person knows that parasitic capacitances occur not only on the gate side but also on the bulk side does not justify a different assessment. According to NKEP1, the resistor arrangement shown in Figure 6c does not serve to reduce parasitic capacitances, but to reduce leakage currents between the voltage source of the control signal and the gate terminal.

73 The fact that the skilled person is aware that the use of individual large resistors in combination with an additional common resistor requires less space, which is also explained in NKEP1, did not give the skilled person sufficient reason to provide the arrangement of resistors shown in NKEP1 for transistors with four externally connected terminals on the bulk and gate side. Against the background

of the task of improving the reliability of a switch with transistors with four terminals, the person skilled in the art will only consider space-saving measures if these are not associated with a reduction in safety.

74 cc) No further suggestion arises from NKD1.

75 It is true that NKD1 with Figure 3 shows a schematic diagram of a switch with transistors having four terminals. In these transistors, not only the gate terminal but also the bulk terminal is "floated" by the arrangement of a resistor between these terminals and the voltage source for the control signal on the gate side and the voltage source on the bulk side, respectively.

76 However, contrary to what the appeal suggests, there is no suggestion from NKD1 to provide an additional common resistor on the gate side and the bulk side according to features 1.3 and 1.5, which is coupled to the plurality of resistors and the respective voltage source.

77 It can remain open whether the Patent Court's assumption that fundamental differences between the bulk side and the gate side prevent such further development is correct.

78 In any case, there is no suggestion for this because, as already explained above, NKD1 explicitly teaches the use of large, individual resistors and reasons that this avoids signal coupling between the transistors connected in series.

79 Against this background, contrary to what the appeal suggests, it can also not be assumed that a reason arose from the NKD1 to test a resistance topology with additional resistances.

80 dd) The other state of the art does not give rise to any further suggestions.

81 IV. The decision on costs follows from Sec. 121 (2) Patent Law and Sec. 97 (1) Code of Civil Procedure (ZPO).

Deichfuß Hoffmann Marx

Rombach Crummenerl

Lower court:
Federal Patent Court, decision of 09.12.2020 - 5 Ni 12/18 (EP) -