Machine Translation

# FEDERAL SUPREME COURT

## IN THE NAME OF THE PEOPLE

## JUDGMENT

X ZR 129/21

Pronounced on:
August 29, 2023
Zöller
Judicial Employee
as Clerk of the Court
Registry

in the patent nullity case

ECLI:EN:BGH:2023:290823UXZR129.21.0

The X. Civil Senate of the Federal Supreme Court, at the oral hearing on August 29, 2023, by the Presiding Judge Dr. Bacher, Judges Hoffmann and Dr. Deichfuß, Judge Dr. Marx, and Judge Dr. Crummenerl,

ruled as follows:

The appeal against the judgment of the 2nd Senate (Nullity Senate) of the Federal Patent Court of October 14, 2021, is dismissed at the defendant's expense.

By law

Facts of the Case:

1 The defendant is the owner of European patent 2 499 640 (patent in suit), which was granted with effect for the Federal Republic of Germany, was filed on November 11, 2010, claiming a priority of November 12, 2009, and relates to operating a memory device.

2 Claim 1, to which seven further claims are referred back, reads in procedural language:

> 1. An apparatus comprising:
> a bit cell (102, 202) coupled to a first bit line (108, 208), a second bit line (110, 210), and a wordline (106, 206) that is responsive to a wordline driver (138, 238); a sense amplifier (116, 216) coupled to the first bit line (108, 208) and to the second bit line (110, 210); a timing circuit (232) configured to generate a first signal (101, 201) and a second signal (103, 203); a loop circuit (114, 214) configured to provide a sense amplifier enable signal (105, 205) to the sense amplifier (116, 216) in response to receiving the first signal (101, 201); and a wordline enable circuit (112, 212) configured to provide a wordline enable signal (113, 213) to the wordline driver (138, 238) in response to receiving the second signal (103, 203), wherein the loop circuit (114, 214) is operative to receive the first signal (101, 201) before the wordline, enable circuit (112, 212) receives the second signal (103, 203) and is programmable to adjust a delay of the sense amplifier enable signal (105, 205).

3 Claim 9, to which five further claims are referred back, protects a method with corresponding features, claim 15, to which one further claim is referred back, protects a computer-readable memory medium with corresponding instructions.

4 The plaintiff argued that the subject matter of the patent in suit was not patentable. The defendant has defended the patent as amended and, in the alternative, in nine amended versions.

5 The Patent Court declared the patent in suit invalid. In its appeal against this decision, the defendant continues to pursue its main and auxiliary requests of the first instance. The plaintiff opposes the appeal.

Reasons for Decision:

6 The admissible appeal is unfounded.

7 I. The patent in suit is related to operating a memory device.

8 1. According to the description of the patent in suit, the operating time of a portable personal computing, such as a cellular telephone, can be increased between recharging or replacing the batteries by reducing the power consumption. Reducing the supply voltage would typically result in lower power consumption. However, some electronic elements may then operate at a slower speed (para. 3).

9 The slower speed could have an impact on the functionality of certain circuits in the electronic device. For example, some memory devices, such as SRAMs (static random access memory), would read the data values stored in their bit cells by precharging a pair of bit lines coupled to the bit cell and then discharging one of the bit lines depending on the stored data value. A sense amplifier coupled to the bit lines would compare the voltages on the bit lines and generate an output indicating the data value at the bit cell. On the one hand, the sense amplifier must wait long enough for the voltage between the two bit lines to be large enough to obtain a reliable result for the data value. On the other hand, to avoid unnecessary power consumption, any unnecessary delay must be avoided (para. 4).

10 2. Against this background, the patent in suit, as the Patent Court correctly assumed, concerns the technical problem of operating a memory device within a range of operating voltages with the lowest possible power consumption.

11 3. To solve this, claim 1 proposes a device whose features can be divided as follows:

12

| | An apparatus comprising: | Eine Vorrichtung, umfassend: |
|---|---|---|
| 1 | a bitcell (102, 202) coupled to a first bit line (108, 208), a second bit line (110, 210), | eine Bitzelle (102, 202), die gekoppelt ist an eine erste Bitleitung (108, 208), eine zweite Bitleitung (110, 210), |
| 2 | and a wordline (106, 206) that is responsive to a wordline driver (138, 238); | eine Wortleitung (106, 206), die auf einen Wortleitungstreiber (138, 238) anspricht; |
| 3 | a sense amplifier (116, 216) coupled to the first bit line (108, 208) and to the second bit line (110, 210); | einen Abfühlverstärker (116, 216), der an die erste Bitleitung (108, 208) und an die zweite Bitleitung (110, 210) gekoppelt ist; |
| 4 | a timing circuit (232) configured to generate a first signal (101, 201) and a second signal (103, 203); | eine Zeitsteuerungsschaltung (232), die konfiguriert ist, um ein erstes Signal (101, 201) und ein zweites Signal (103, 203) zu generieren; |
| 5 | a loop circuit (114, 214) configured to provide a sense amplifier enable signal (105, 205) to the sense amplifier (116, 216) in response to receiving the first signal (101, 201); | eine Schleifenschaltung (114, 214), die konfiguriert ist, um ein Abfühlverstärkeraktivierungssignal (105, 205) an den Abfühlverstärker (116, 216) in Reaktion auf das Empfangen des ersten Signals (101, 201) zu liefern; |
| 6 | and a wordline enable circuit (112, 212) configured to provide a wordline enable signal (113, 213) to the wordline driver (138, 238) in response to receiving the second signal (103, 203), | eine Wortleitungsaktivierungsschaltung (112, 212), die konfiguriert ist, in Reaktion auf das Empfangen des zweiten Signals (103, 203) ein Wortleitungsaktivierungssignal (113, 213) an den Wortleitungstreiber (138, 238) zu liefern. |
| 7 | wherein the loop circuit (114, 214) is operative to receive the first signal (101, 201) before the wordline enable circuit (112, 212) receives the second signal (103, 203) and is programmable to adjust a delay of the sense amplifier enable signal (105, 205) | Die Schleifenschaltung (114, 214) ist betreibbar zum Empfangen des ersten Signals (101, 201), bevor die Wortleitungsaktivierungsschaltung (112, 212) das zweite Signal (103, 203) empfängt, und programmierbar, um eine Verzögerung des Abfühlverstärkeraktivierungssignals (105, 205) anzupassen. |

13 4. The claim requires further discussion.

14 a) Features 1 to 3 describe the basic elements of a memory system which is explained in the patent in suit by means of an SRAM consisting of six transistors and illustrated, inter alia, by Figure 2 reproduced below.

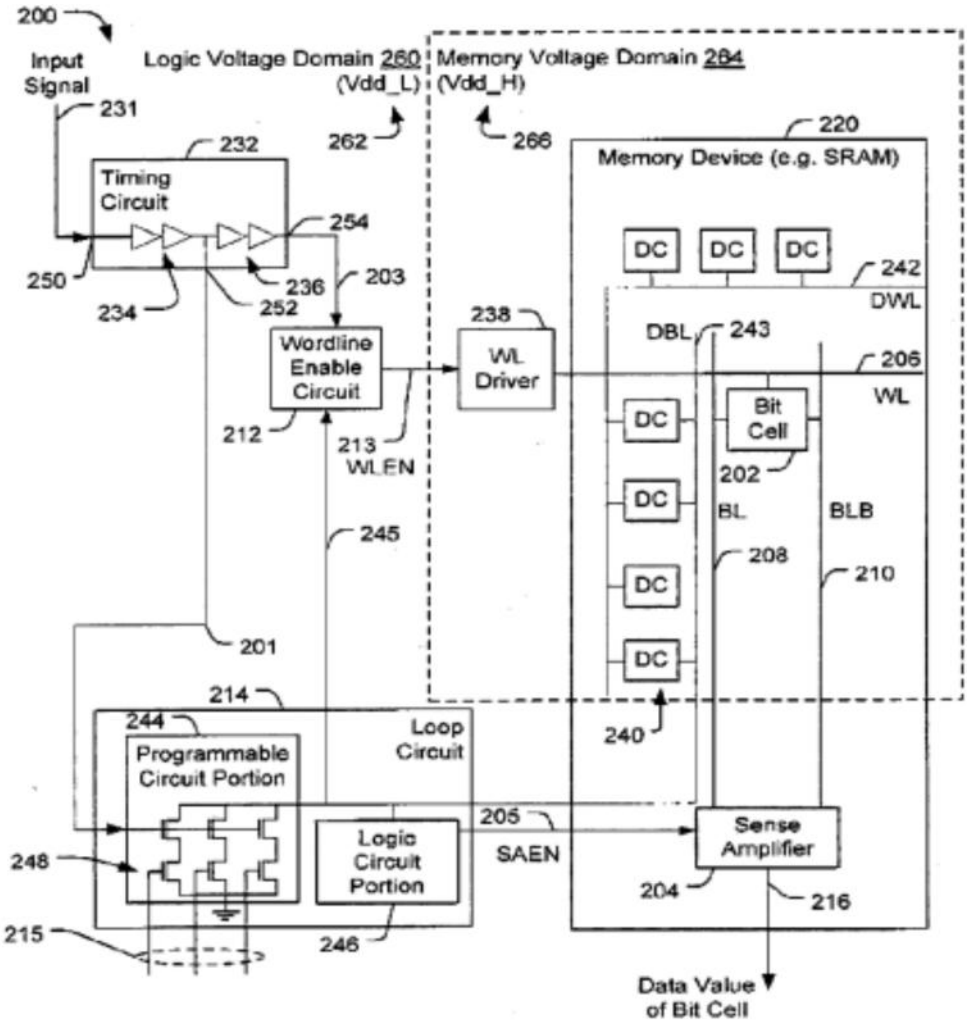


***FIG. 2***

15 Each bit cell (202) is coupled to two bit lines (208, 210) which are used for write and read access. It is also connected to a wordline (206) whose activation enables access.

16 For writing, one of the two bit lines is set to the operating voltage. Depending on the activated line, the cell stores the value 0 or 1.

17 For readout, both bit lines are charged to about half the operating voltage. Activating the wordline discharges one of the two bit lines and raises the other to a higher voltage level. A sense amplifier (204) connected to the bit lines determines the voltage between the two bit lines. If this exceeds a certain threshold value, the result is evaluated as 0 or 1, depending on the polarity.

18 The build-up of the voltage between the bit lines takes a certain time. If the sense amplifier is activated too early, this can lead to a data value not (yet) being readable or the measurement result being evaluated as invalid. Activating too late can increase the energy consumption, because this is time-dependent and increases with rising voltage.

19 b) To enable reading, feature 5 provides a loop circuit to enable the sense amplifier and feature 6 provides a circuit to enable the wordline.

20 c) The two signals that the timing circuit (232) must be capable of generating according to feature 4 are used to control the sense amplifier and the wordline according to features 5 and 6.

21 aa) It follows from the requirement formulated in feature 4 that there must be a first and a second signal that the two signals must be separate from each other.

22 This is confirmed by the requirement in feature 7 that the loop circuit which provides the signal to enable the sense amplifier according to feature 5 must be able to receive the first signal before the wordline enable circuit receives the second signal.

23 bb) Contrary to the opinion of the appeal, however, it does not follow from this that the first signal must necessarily be generated before the second.

24 (1) As the appeal does not fail to recognize in its approach, the terms "first" and "second" do not necessarily imply a chronological order.

25 This pair of terms is usually used to distinguish two different objects from each other. A certain distinguishing criterion is not yet necessarily given with it.

26 Against a different understanding in the context of the patent in suit is the fact that the description uses the pair of terms not only in connection with the two signals generated in the timing circuit, but also in connection with the outputs at which these signals are made available (para. 22: first output 252, second output 254).

27 (2) The fact that circuit (232) is designated as a timing circuit does not lead to a different assessment, contrary to the view of the appeal.

28 It follows from this concept that the time at which the signals are generated must be controllable. However, this does not necessarily mean that the first signal must be generated before the second.

29 (3) A time sequence for generating the signals also does not result from feature 7.

30 (a) Feature 7 specifies the order in which the two signals are received by the loop circuit and the wordline enable circuit, respectively.

31 This sequence does not necessarily have to correspond to the sequence of generation. On the contrary, the order of reception can also be influenced by the fact that the signals are delayed to varying degrees after their generation.

32 (b) No narrower understanding results from the embodiment example according to Figure 2.

33 In this embodiment, an input signal (231) is supplied to the timing circuit (232) via an input (250), which may be, for example, a clock signal. This signal is delayed at a first set of gates (234) to produce the first signal (201) at a first output (252). A second set of gates (236) generates a second signal (203) at a second output (254). This embodiment may be replaced by other embodiments according to the description, in which the first signal occurs before the second signal (para. 22).

34 All these embodiments have in common that the timing circuit generates the first signal earlier in the sense that it is applied to the associated output before the second signal. However, this particular embodiment has not been reflected in claim 1. The fact that the two signals in the example described are generated by different delays of the input signal rather confirms that it is not the order of generation that is decisive, but the order in which the two signals are received at the decisive points, i.e., at the loop circuit and at the wordline enable circuit. From this point of view, it is irrelevant whether a different delay already takes place within a unit designated as a timing circuit or in downstream components.

35 cc) Features 4 to 7 also do not specify the manner in which the two signals are further processed.

36 Features 5 and 6 provide in this respect that receiving the first or second signal leads in each case to the transmission of a further signal which enables the sensing amplifier or the word line. The modalities under which these further signals are generated are not defined in detail. In particular, it cannot be ruled out that these signals are only generated or sent after a certain period of time after the first or second signal has been received. For the sense amplifier activation signal, feature 7 even makes the possibility of such a delay mandatory.

37 d) According to feature 7, the loop circuit must also be programmable in order to be able to adjust the delay of the sense amplifier enable signal.

38 aa) The time between receiving the first signal by the loop circuit and receiving the second signal by the wordline enable circuit can be used as an additional means to enable the sense amplifier at the most favorable time.

39 According to the description of the patent in suit, this is advantageous in particular if the enabling of the sense amplifier takes more time than reaching the threshold value required for a readout on the bit lines after enabling the wordline.

40 bb) This relationship is illustrated in more detail in the description on the basis of the embodiment example according to Figure 2.

41 (1) The loop circuit (214) is coupled to a dummy bit line (243) and includes a programmable circuit portion (244) and a logic circuit portion (246). It may be

programmed to provide a substantially constant delay between enabling the wordline signal and enabling the sense amplifier enable signal.

42 In one embodiment, the programmable circuit portion (244) includes multiple discharge devices (discharge devices 248) coupled to the dummy bit line (243) and allowing the discharge rate of the precharged dummy bit line to be adjusted (para. 26).

43 The logic circuit portion (246) responds to the discharge of the dummy bit line (243) and generates the sense amplifier enable signal (205). The components of the logic circuit portion (246) may operate at reduced speed when the supply voltage drops. Therefore, the programmable circuit portion (244) may be controlled so that the delay between enabling the wordline and enabling the sense amplifier nevertheless remains substantially constant (para. 27).

44 (2) This procedure is illustrated in Figure 3 below.

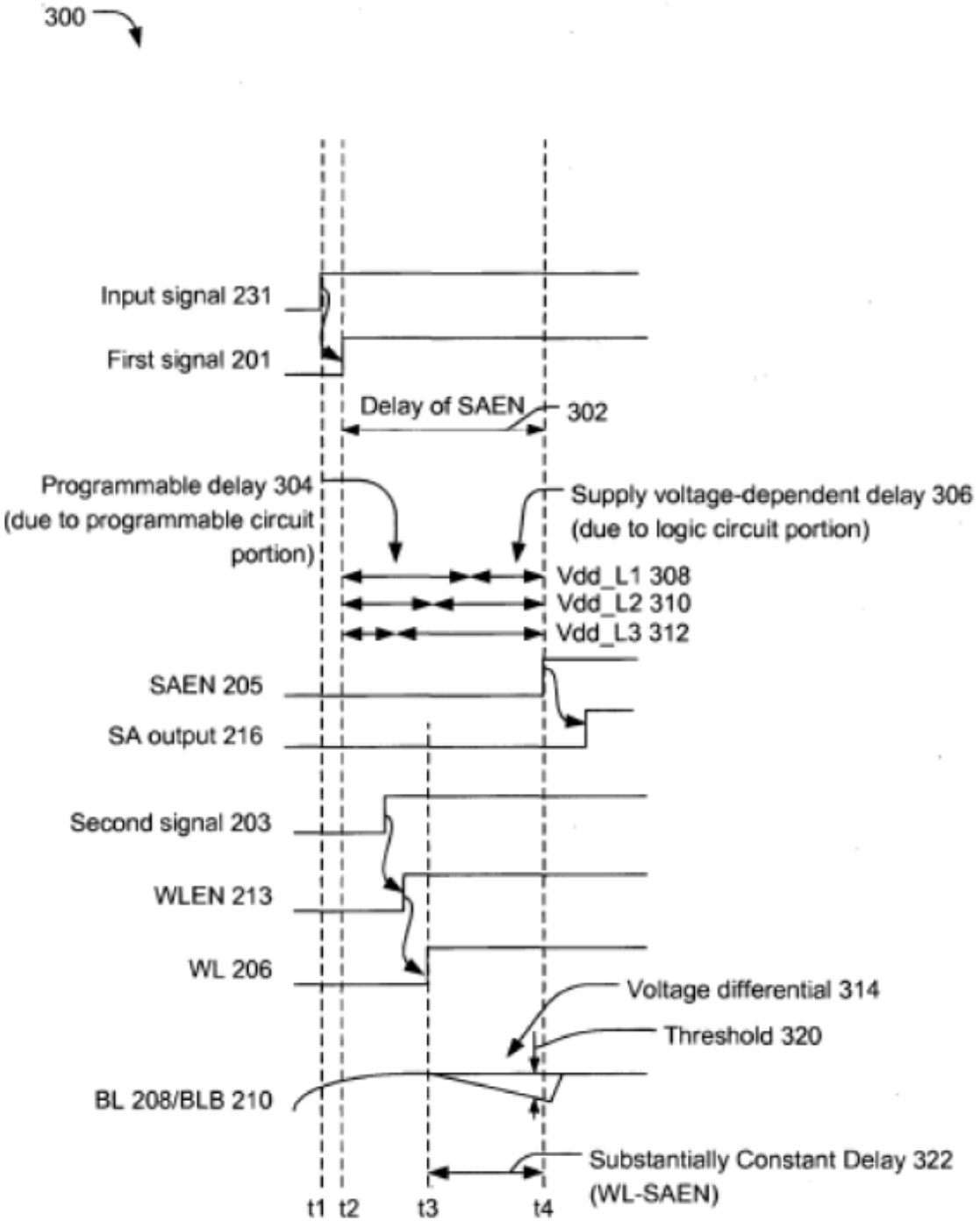
300
Input signal 231
First signal 201
Delay of SAEN
302
Programmable delay 304
(due to programmable circuit portion)
Supply voltage-dependent delay 306
(due to logic circuit portion)
Vdd_L1 308
Vdd_L2 310
Vdd_L3 312
SAEN 205
SA output 216
Second signal 203
WLEN 213
WL 206
Voltage differential 314
Threshold 320
BL 208/BLB 210
Substantially Constant Delay 322
(WL-SAEN)
t1
t2
t3
t4

*FIG. 3*

45 At time t1 the input signal (231) is generated, at time t2 the first signal (201) (para. 28).

46 At time t3, the word line (206) is activated, in response to the second signal (203) and the activation signal (213) generated in response thereto (para. 30).

47 At time t4, the signal (205) to enable the sense amplifier is generated in response to the first signal (201). The delay period (302) between this time and the time t2 at which the first signal (201) occurs is kept substantially constant by the programming. This period consists of the time period (306) required by the logic circuit portion to generate the enable signal (205) and an additional time period (304), the duration of which can be programmed. When lowering the supply voltage (Vdd) from L1 to L3, the time period (306) increases due to the reduced operating speed of the logic circuit portion. To keep the total duration constant, the programmable delay (304) is decreased accordingly (para. 29).

48 The arrival of the first signal (201) already at time t2 - i.e. before the arrival of the second signal (203) - makes it possible to keep the total duration and the delay (322) between times t3 and t4 constant even at the lowest supply voltage (Vdd_L3).

49 (3) This procedure can be particularly advantageous if only the supply voltage of the loop circuit (214) is reduced, but the supply voltage for the bit cells is higher.

50 The use of different supply voltages within the overall system is explicitly addressed in the description of the patent in suit (para. 20).

51 cc) However, the approach illustrated in Figures 2 and 3 has not been reflected in feature 7.

52 Referring to the context of Figure 3, feature 7 simply specifies that the time t2 is before the arrival of the second signal (203) and that the time period (304) can be adjusted by programming.

53 It is not necessarily predetermined that the delay period (322) is kept constant, that enabling of the logic circuit portion - not necessarily provided for in the claim - is possible before the arrival of the second signal (203), and that the adjustment is based on the delay that occurs when the sense amplifier is enabled.

54 Nor is it specified that an adjustment due to a reduction of the supply voltage must be possible during operation of the claimed device.

55 II. The Patent Court gave the following main reasons for its decision - insofar as it is still of interest in the appeal proceedings:

56 The subject matter of claim 1 as granted and in the versions of the auxiliary requests was not new compared to the teaching in the publication by Amrutur and Horowitz (A Replica Technique for Wordline and Sense Control in Low-Power SRAM's, in: IEEE Journal of Solid-State Circuits, Vol. 33, No. 8, 1998, pp. 1208 to 1219; K6).

57 K6 discloses a memory circuit for an SRAM in which the timing of the signals is adapted to different operating conditions, using dummy memory cells with dummy bit lines and dummy wordlines, not unlike the patent in suit.

58 The branch shown in K6 in Figure 10 with two inverters (B1, B2) and the NOR element arranged in front of it represent a timing circuit that generates a

first and a second signal, with the first signal being enabled before the second signal. The operation of the timing circuit is in this respect identical to the embodiment example according to Figure 2 of the patent in suit. The NAND element shown in Figure 9 of K6 in the left part of the circuit, which has as input a second signal (bs) and a further signal (gwl), represents a wordline enable circuit. The inverting driver shown in the middle part of the circuit (upper two transistors) is a wordline driver. The circuit B3/B4 shown in Figure 10 with replica wordline (fwl), replica bit line, dummy cells and current sources as well as the inverters F1, S2, S3 form a loop circuit.

59 In the circuit shown in Figure 8, a dummy bit line (replica bit line) to which dummy memory cells are connected is discharged for delay. Since the conditions for this bit line are the same as for all other bit lines, it is possible to measure how the individual components behave under different conditions and what times result for discharging the bit lines. Since the sense amplifier used for this purpose requires only a fraction of the operating voltage as a signal, only a fraction of the discharge is required for recognition of the memory contents. This fraction would have to be set for the "replica bit line" (rbl) and the subsequent logic circuit. While this is done in the first example (capacitance ratioing) by shortening the replica bit line compared to the other bit lines, this is done in the second example with a complete bit line that is discharged with the aid of several dummy memory cells acting as current sources.

60 The timing circuit would thereafter be configured in accordance with feature 4 to generate a first signal (right branching line to circuit B3/B4) and a second signal (bs). The loop circuit would be configured in accordance with feature 5 to provide a sense amplifier enable signal (signal "sense" after inverter S3) to the sense amplifier (sense amps) in response to receiving the first signal (signal on the right branching line after the NOR gate). Referring to feature 6,

the wordline enable circuit is configured to provide an enable signal (output signal of the NAND circuit on the line above the lower two transistors in the left portion of the circuit in Fig. 9) to the word line driver (center portion of the circuit in Fig. 9) in response to receiving the second signal (bs). Finally, the loop circuit as defined in feature 7 is operable to receive the first signal (signal on right branching line) before the wordline enable circuit (left portion in Fig. 9) receives the second signal (bs), and is programmable with the programmable current sources to adjust a delay of the enable signal (sense) for the sense amplifier.

61 The subject-matter of the auxiliary requests was also disclosed in K6. Even if feature 8 added to auxiliary requests 2 and 2a were not considered disclosed, the subject matter of these auxiliary requests would be obvious to a person skilled in the art, a professionally experienced electrical engineer or hardware-oriented computer scientist with a technical college or university degree in charge of the development of SRAM memory devices, with good knowledge in the field of design and operation of semiconductor memories for information storage, in obvious combination with US application 2007/0002636 (K13) or the textbook edited by Wang and Naffziger (Adaptive Techniques for Dynamic Processor Optimization, Theory and Practice, 2008, pp. 134 to 137; K15).

62 III. This assessment stands up to scrutiny in the appeal proceedings.

63 1. The Patent Court correctly held that the subject matter of claim 1 as granted is fully disclosed in K6.

64 a) K6 deals with the adaptation of SRAMs to lower supply voltages.

65 aa) K6 states that in order to save energy, SRAMs with lower supply voltages are continuously being developed. The threshold values for the voltage do not decrease to the same extent. Therefore, delay variability is expected to increase as development continues. This would lead to a greater power loss on the bit lines and to losses in speed (p. 1208, left column).

66 Bit line swings could be limited by using high impedance loads and pulsing wordlines. To further reduce the required power, the pulse width could be set just wide enough to ensure minimal development of bit line swings. This, he said, can be achieved by using a precise pulse generator that adapts to the bit line delay. Low-power SRAMs also used clocked sampling amplifiers to limit sampling power (p. 1208, left/right column).

67 Basically, the clock path and the data path would have to match. Delay variations would be dominated by delay of the bit lines. A corresponding delay margin for the sampling clock path would reduce the performance (p. 1208, right column).

68 To reduce these negative effects, K6 proposes to use replica circuits to generate a reference signal whose delay follows that of the bit lines. This signal is used to generate a sampling clock with minimum slack time and to achieve pulse widths for the word lines that limit the voltage differences of the bit lines (Abstract).

69 bb) An example of a control circuit suitable for this purpose is shown in Figure 10 reproduced below.

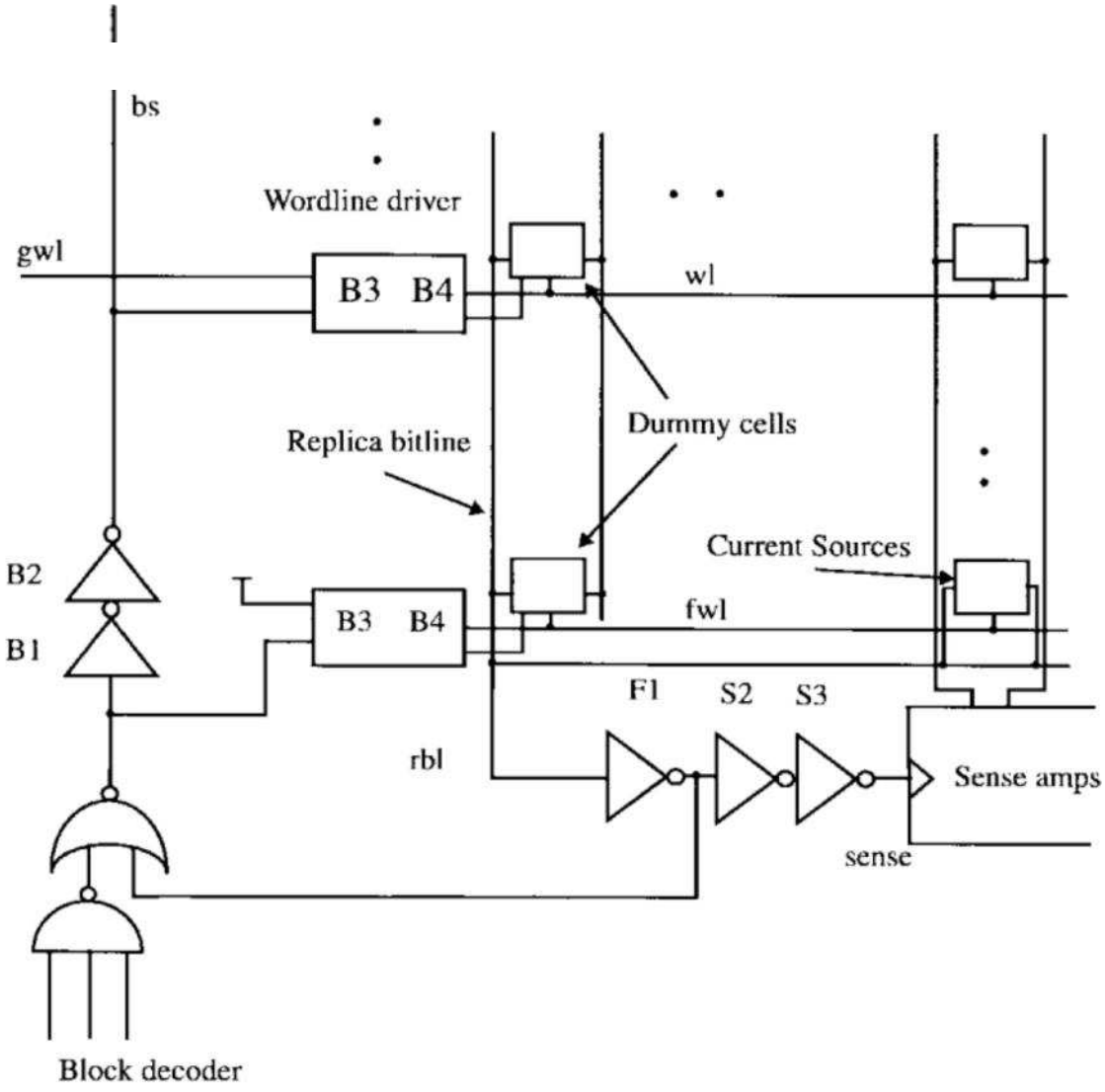


Fig. 10. Control circuits for current-ratio-based replica structure.

70 The block decoder includes a NOR element used as a signal input for time signals. After this the signal branches into a first signal which branches off to the right and into a second signal which goes to two inverters (B1, B2) and is delayed by them.

71 (1) The second signal continues to a wordline driver (wordline driver B3, B4).

72 According to Figure 9 reproduced below, this can have a circuit part (left) which is the input for the second signal (bs) activating the wordline (wl) when the circuit is selected by the further signal (gwl). The middle part of the circuit drives the wordline (wl) with its transistors.

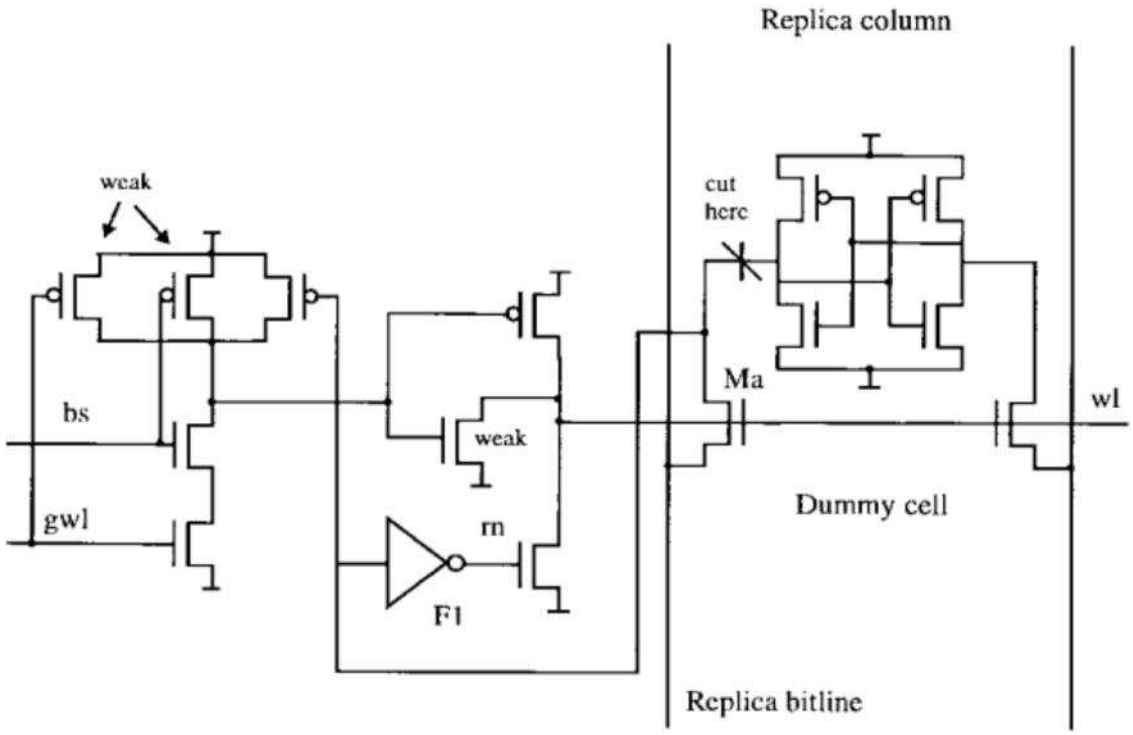


Fig. 9. Skewed wordline driver.

73 (2) The first signal passes through an always-selected wordline driver to a replica wordline that enables a delay circuit. This circuit is shown in Figure 8 reproduced below.

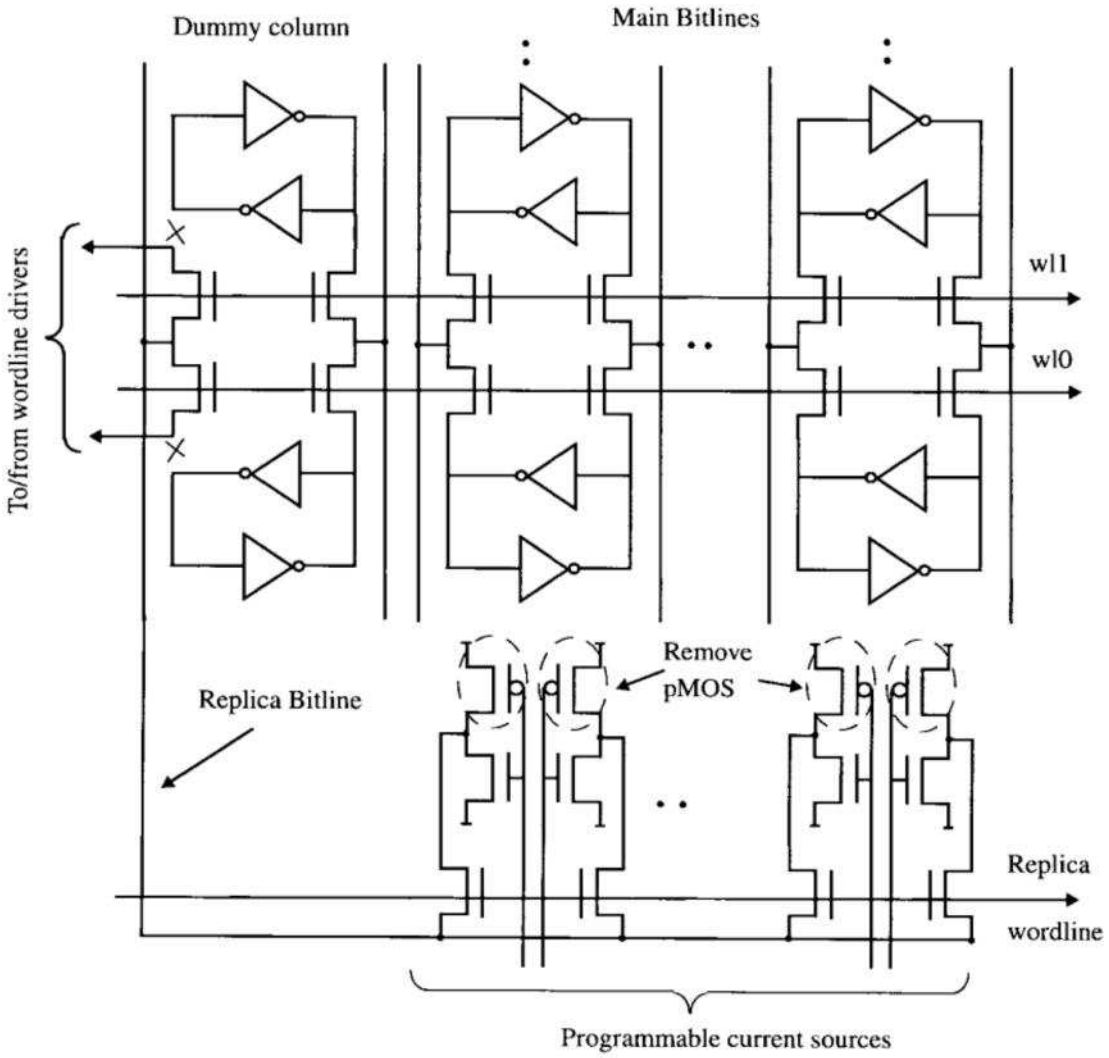


Fig. 8. Current-ratio-based replica structure.

74 The sense amplifier used in this area requires only a fraction of the operating voltage for readout. Therefore, only a corresponding fraction of discharge is required on the replica bit line to be able to recognize the memory contents.

75 The adjustment required for this is achieved in one example (capacitance ratioing) by shortening the replica bit line relative to the other bit lines. The time span between enabling of the replica delay cell to the discharge of the replica bit line corresponds very closely to that on the main bit line. A complete match can be achieved by fine tuning based on simulations.

The output signal of the replica delay cell is fed into a buffer chain that starts local scanning. It is simultaneously fed back to the block decoder to reset the block select signal. In this way, the pulse width of the wordline pulse is determined by the width of the block selection signal. The delay of the buffer chain to drive the scan signal is compensated by enabling the replica delay cell with the non-buffered block select signal (p. 1210).

76 In the example shown in Figure 8, the replica bit line is discharged to improve access times using multiple dummy memory cells acting as current sources. This increases the speed at which the replica bit line is discharged, achieving the same effect as decreasing the discharge capacity (p. 1213 left column). In Figure 8, the current sources are referred to as programmable current sources.

77 The dummy word line driver is activated by the unbuffered block selection fwl. The replica bit line is detected by F1 and buffered to drive the sampling signal. When the delay of the replica bit line matches the bit line delay and the delay of F1, S2, S3 is equal to that of B1, B2, the sampling clock triggers at the time when the difference of the voltages of the bit line has the desired magnitude. If the delay of B1, B2 coincides with the delay of generating rn (Fig. 9) from the replica bit line, the word line pulse width is the minimum value required to generate the required voltage difference of the bit lines (p. 1214 li. sp.).

78 b) K6 thus discloses features 1, 2, 3, 5, and 6, as the appeal also does not doubt.

79 Contrary to the opinion of the appeal, however, the NAND gate shown in Figure 10, bottom left, functioning as a block decoder, is not to be regarded as a wordline enable circuit within the meaning of feature 6. Rather, as the Patent Court rightly assumed, this function is realized by the component (B3) which is also designed as a NAND element.

80 As the appeal correctly asserts in its approach, the wordline enable circuit according to feature 6 has the function of addressing the wordline on the basis of an input signal by means of a wordline driver. However, this input signal must be one of the two signals generated by the timing circuit provided in feature 4. Two different signals are generated in the circuit shown in Figure 10 only by the NOR gate arranged after the block decoder and the inverters B1 and B2 arranged on the signal path leading upward. Consequently, only the element B4 downstream of B3 functions as a wordline driver in the sense of feature 6 in K6.

81 The fact that in Figure 10 both B3 and B4 are designated as wordline drivers does not lead to a different assessment. In this respect, the nomenclature specified by the patent in suit, which distinguishes between enable circuit and driver, is decisive. According to this classification, B3 belongs to the enable circuit for the reasons stated.

82 c) Contrary to the view of the appeal, feature 4 is also disclosed in K6.

83 aa) As has already been explained above, in the circuit shown in Figure 10 the signal coming in at the bottom left via the block decoder and the NOR element is divided into a first signal which is fed to the loop circuit without delay and a second signal which goes to the wordline enable circuit with a delay through inverters B1 and B2.

84 Thus, as the Patent Court correctly pointed out, two different signals are generated, the first of which is even the temporally preceding one.

85 bb) The fact that the first signal before the sensing amplifier is also delayed by an amplifier (F1) and two further inverters (S1, S2) and that this delay, according to the explanations in K6, should preferably correspond to that caused by the inverters B1 and B2 (p. 1214, left column), does not lead to a different assessment, contrary to the opinion of the appeal.

86 As has also already been explained, the patent in suit also provides in feature 7 that the first signal arriving in the loop circuit only leads to the generation of a sense amplifier enable signal after an (adjustable) delay. Such an additional delay is caused in K6 by the components F1, S2 and S3.

87 d) K6 also discloses feature 7.

88 As the Patent Court correctly pointed out on the merits, the splitting of the signal after the NOR gate and the delay by inverters B1 and B2 of the signal leading to the wordline enable circuit cause the signal led to the loop guide to arrive first. The circuit shown in Figure 8 causes the subsequent time period until the sense amplifier enable signal is triggered to be determined by the time period required to discharge the dummy bit line. This time period can be influenced by the programmable current sources.

89 Thus, feature 1.7 is fully disclosed.

90 aa) Contrary to the view of the appeal, it is irrelevant whether the circuits disclosed in K6 serve only to detect delays in the discharge process of the bit lines and not to detect delays on the sense amplifier path.

91 As explained above, detection of delays on the sensing amplifier path according to feature 7 is not mandatory.

92 bb) The fact that the Patent Court considered only the embodiment with programmable current sources shown in Figure 8 to be novelty-damaging, but not the embodiment with shortened dummy bit line described in K6 as having the same function, does not justify a contradiction.

93 The Patent Court rightly saw the decisive difference in the present context in the fact that programmability is expressly disclosed for the embodiment with current sources, whereas it is not disclosed for the embodiment with a shortened dummy bit line.

94 cc) The statements contained in K6, according to which all outputs of the memory cells acting as current sources are connected to each other and simultaneously discharge the replica bit line (p. 1213, left column, bottom), do not lead to a different assessment.

95 However, it can be seen from these explanations that once the current sources used have been specified - just as after a shortening of the bit line - there are no additional adjustment possibilities. The statement that the current sources are programmable, however, refers to the preceding phase of the adjustment. For this K6 states at the same place, by connecting n current sources to the replica bit line their slew rate can be adjusted to n times the slew rate of the main bit line. This discloses a possibility for adjustment by programming, as provided by feature 7.

96 2) The Patent Court was correct in its conclusion that the subject-matter defended by auxiliary requests 1 to 4 is also not patentable.

97 a) The subject matter defended by auxiliary request 1 is fully disclosed by K6.

98 (aa) As amended by auxiliary request 1, feature groups 4 and 7 are worded as follows (amendments are highlighted):

> 4. a timing circuit (232) configured to generate a first signal (101, 201) and a second signal (103, 203) in response to an input signal (231),
>
> 4.1 wherein the input signal (231) is a clock signal;
>
> 4.2 and wherein the first signal is activated prior to the second signal;
>
> 7. wherein the loop circuit (114, 214) is operative to receive the first signal (101, 201) before the wordline enable circuit (112, 212) receives the second signal (103, 203)
>
> 7.1 whereby the first signal initiates the operation of the loop circuit (114, 214) before the second signal initiates the generation of the wordline enable signal,
>
> 7.2 wherein the loop circuit (114, 214) is programmable to adjust a delay of the sense amplifier enable signal (105, 205),
>
> 7.3 whereby the sense amplifier enable signal experiences an increased delay responding to the first signal as the supply voltage of a logic circuit portion of the loop circuit decreases in low power applications.

99 bb) Contrary to the opinion of the appeal, it cannot be inferred from feature 7.3 that the reduction of the supply voltage for a logic circuit portion of the loop circuit must be brought about deliberately and purposefully and must exceed a certain minimum level.

100 Requirements in this respect are not provided for in the wording of feature 7.3. Nor do they result from the requirement that the reduction in voltage must take place in a low voltage mode (low power application). This requirement is not only fulfilled if the voltage drops due to a change to an operating mode with lower voltage, but also if fluctuations occur within such a mode.

101 cc) The disclosure of the amended feature group 4 and of feature 7.1 by K6, as found by the Patent Court, is rightly not doubted by the appeal.

102 In particular, the Patent Court correctly concluded with regard to features 4.2 and 7.1 that because of the inverters B1 and B2 provided in the timing circuit, the second signal is delayed and thus enabled after the first signal (for the further signal path).

103 dd) Feature 7.3 is also disclosed, contrary to the view of the appeal.

104 As the Patent Court correctly pointed out, the delay that is supposed to increase as the supply voltage of a logic circuit component in the loop circuit decreases is the delay designated by reference 306 in Figure 3 of the patent in suit, because only this delay increases as the supply voltage decreases, while the programmable delay 304 decreases under the same conditions.

105 Against this background, the Patent Court rightly came to the conclusion that the effect provided for in feature 7.3 occurs automatically in the event of voltage fluctuations during operation, as is also stated in the description of the patent in suit.

106 b) There is no different assessment for auxiliary request 1a.

107 aa) According to auxiliary request 1a, which builds on auxiliary request 1, feature group 7 reads as follows (changes from auxiliary request 1 are highlighted):

7. wherein the loop circuit (114, 214) is operative to receive the first signal (101, 201) before the wordline enable circuit (112, 212) receives the second signal (103, 203)
   7.1 whereby the first signal initiates the operation of the loop circuit (114, 214) before the second signal initiates the generation of the wordline enable signal,
   7.4 so that a delay of the sense amplifier enable signal (105, 205) may be adjusted to accommodate a delay within the loop circuit (114, 214) due to a supply voltage value,
   7.3" wherein the delay within the loop circuit (114, 214) is an increased delay as the supply voltage of a logic circuit portion of the loop circuit (114, 214) decreases in low power applications,
   7.2 wherein the loop circuit (114, 214) is programmable to adjust ~~a~~ the delay of the sense amplifier enable signal (105, 205).

108 bb) The added feature 7.4, in combination with the reformulated feature 7.3", makes it clear that the adjustment of the delay should take into account an increase in the delay due to a reduction in the supply voltage of a logic circuit portion of the loop circuit.

109 Even with these formulations, however, it is not specified in what way the adjustment is to be made. In particular, it is not specified that the delay is to be adjusted because it occurs only in the loop circuit or in a logic domain, but not in the memory cells, and the compensation must therefore be made by shortening another time period.

110 cc) On this basis, the Patent Court rightly concluded that auxiliary request 1a is not to be assessed differently from auxiliary request 1.

111 c) The subject matter defended by auxiliary requests 2 and 2a is also not patentable.

112 (aa) Auxiliary requests 2 and 2a each add the following feature to the subject matter of auxiliary requests 1 and 1a, respectively:

> 8. wherein the wordline driver (238) and the bit cell (202) exist in a memory voltage domain (264), while other components of the system (200) exist in a logic voltage domain (260).

113 bb) Contrary to the opinion of the Patent Court, it is not sufficient for the realization of this feature if the circuit can be divided abstractly into individual voltage ranges. Rather, the circuit must be designed in such a way that there are at least two areas that can actually be operated with different supply voltages. On the other hand, as the Patent Court correctly assumed, it is not necessary that use is made of this possibility.

114 cc) Thus, feature 8 is not disclosed in K6.

115 The possibility of operating different areas of the circuit with different voltages is not disclosed in K6. The fact that abstract domains can be formed according to the Patent Court's findings is not sufficient for this.

116 dd) The contested decision is, however, supported in this respect by the auxiliary consideration that, starting from K6, it was obvious to operate the two areas with different supply voltages, as is disclosed in K13 and K15, for example.

117 As the appellant rightly argues, K6 aims to reduce energy consumption by lowering the supply voltage. In this regard, it can be seen from K13 and K15 that the reliability of the memory is no longer given if the voltage in the memory portion falls below a certain value, whereas a further reduction is possible in the logic portion (K13 para. 5 et seq.; K15 p. 134 para. 6.3).

118 Based on this, there was reason to divide the circuit into two voltage ranges with different supply voltages for the memory portion and the logic portion also for the design disclosed in K6, so that a further reduction of the voltage for the logic portion is possible.

119 The circumstance cited by the appeal that it would not make sense with such a change to match the delay through components F1, S2 and S3 to that through gates B1 and B2 as proposed in K6 does not lead to a different assessment. A delay in the sense amplifier path due to a lower voltage in the logic portion may indeed lead to additional problems. However, with the instruction to match the delays in the individual components and the use of programmable current sources, K6 also provides approaches to address these problems.

120 The fact that K6 does not disclose compensation for additional delays due to a reduction in the supply voltage in the logic portion by reducing the delay that can be adjusted by programming does not lead to a different assessment, if only because feature group 7 also does not necessarily provide for adjustment in this way.

121 d) The Patent Court was in any case correct in denying the patentability of the subject-matter defended by auxiliary requests 3 and 4.

122 aa) The auxiliary requests 3 and 4 add the following feature to claim 1 as granted or as amended according to auxiliary request 1:

> 9. and wherein the loop circuit (114, 214) is further configured to provide a disable signal (245) to the wordline enable circuit to disable the wordline enable signal.

123 bb) Whether this feature is disclosed in K6, as the Patent Court assumed, by the fact that in Figure 9 a deactivation signal runs from the replica bit line via the transistor (Ma) to the upper right transistor of the extended NAND gate, or whether these components belong to the wordline enable circuit, as the appeal suggests, does not require a final decision.

124 As the appellant rightly asserts, a deactivation signal for the wordline originating from the loop circuit is in any case disclosed by Figure 10 and the explanations relating thereto already reproduced above, according to which the inverter F1 outputs a logic 1 after discharging the replica bit line with the consequence that B4 outputs a 0 via the NOR gate, the inverters B1 and B2 and the gate B3 and thus deactivates the wordline.

125 e) The subject matter defended by auxiliary request 5 is also not patentable.

126 (aa) Based on auxiliary request 1, auxiliary request 5 provides for the following changes:

> An apparatus, <u>having various supply voltages,</u> comprising:
> ...
>
> 7.1' whereby the first signal initiates the operation of the loop circuit (114, 214) before the second signal initiates the generation of the wordline enable signal,

in order to give the sense amplifier additional time to adjust for a lower operating voltage,

7.2' wherein the loop circuit (114, 214) is programmable to ~~adjust a delay~~ maintain a substantially constant delay between activation of a wordline signal by the wordline driver (138, 238) and activation of the sense amplifier enable signal (105, 205),

7.3' and wherein the substantially constant delay is substantially independent of a supply voltage of a logic domain.

127 bb) The Patent Court correctly assumed that the new input feature (having various supply voltages) leaves open the number of possible operating voltages and the time of their occurrence. In particular, no restriction to devices whose operating voltages change during operation is to be inferred from it, nor from the amended subsequent features.

128 Accordingly, it is sufficient for the disclosure of this feature to state that the device according to K6 can be operated with the operating voltages 1.0 V, 0.75 V, 0.5 V, 0.45 V, and 0.4 V (p. 1218 Table V).

129 cc) Features 7.2' and 7.3' flesh out the manner in which the delay of the sense amplifier enable signal is adjusted so that the delay between activation of the wordline signal by the wordline driver and the activation of the signal for the sense amplifier remains substantially the same regardless of the supply voltage in the logic domain.

130 If the supply voltage of the logic domain changes, however, a period that is decisive for the total delay changes. Consequently, to keep the delay constant, another time period must be adjusted. This corresponds to the procedure as shown in Figure 3 of the patent in suit.

131 Contrary to the view of the Patent Court, it is not sufficient for programmability within the meaning of feature 7.2' that the programmable components disclosed in K6 can be equipped with software that enables such adaptation of the delay. Rather, the device must already be equipped with hardware and software that provide functions suitable and intended for this purpose.

132 dd) The Patent Court rightly assumed, unchallenged by the appeal, that feature 7.1' is also disclosed with the additional amendments in K6 for the reasons already explained in connection with auxiliary request 1 regarding feature 7.1.

133 ee) The use of different voltages - also in such a way that the memory and logic portions are operated with different voltages - is in any case suggested by K13 and K15 for the reasons explained above.

134 ff) The Patent Court rightly concluded that, based on K6, it was obvious to allow an adjustment of the delay according to features 7.2' and 7.3'.

135 The reduction of the supply voltage in the logic portion leads to an additional delay of the first signal by the inverters F1, S2, S3 shown in Figure 10 with the consequence that the sense amplifier enable signal is also output with an additional delay. To compensate for this delay, K6 provides a suitable compensation mechanism with the programmable current sources already present there.

136 This resulted, as the Patent Court rightly assumed in the result, in the suggestion to also use this adjustment possibility to compensate for an additional delay resulting from the reduction of the supply voltage in the logic portion. The fact that the use of the programmable current sources for an additional delay based on this cause is not disclosed in K6 does not contradict

this. As the Patent Court correctly assumed, K6 discloses the basic idea that the time at which the sense amplifier is activated is of decisive importance. In order to determine the correct point in time for the activation, it is not decisive what the delay to be compensated is based on.

137 f) For auxiliary request 6, which is a combination of auxiliary requests 1, 2, 3 and 5, no different assessment results.

138 (g) Nothing to the contrary applies to auxiliary request 6a.

139 aa) Auxiliary request 6a differs from auxiliary request 6 in that the word "substantially" is omitted in features 7.2' and 7.3' respectively.

140 bb) This concretization does not lead to a different assessment.

141 As explained in connection with auxiliary request 5, starting from K6 it was obvious to use the means for adjusting the delay disclosed there also for compensating delays in the sense amplifier path due to a reduction of the supply voltage in the logic portion. Here it was obvious to keep the total delay as constant as possible.

142 IV. The decision on costs is based on Sec. 121 (2) Patent Law and Sec. 97 (1) Code of Civil Procedure (ZPO).

Bacher Hoffmann Deichfuß

Marx Crummenerl

Lower court:
Federal Patent Court, decision of October 14, 2021 - 2 Ni 15/20 (EP) -